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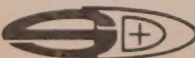


INSTRUCTION MANUAL

MODEL 50
MICROPROCESSOR ANALYZER

SERIAL NO. 04010-7

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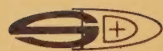
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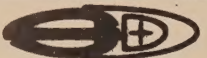
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**Note:**

If AI-6502 is used with the DC-03 cable, pin 37 of the clip must be insulated from the CPU chip, otherwise the cable capacitance may adversely effect the oscillator. This can be done by slipping a piece of "spaghetti" (insulating sleeve) of the right diameter on pin 37 of the clip, and removed when using the DC-03 with other processors.

MODEL 50
MICROPROCESSOR ANALYZER



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A UNIVERSAL INSTRUMENT FOR SOFTWARE/HARDWARE TROUBLESHOOTING

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10 Systron Drive
Concord, California 94518

SUMMARY

A new Microprocessor analyzer has been developed, which is essentially a sophisticated Address and Data Bus Monitor with hardware breakpoint capability. The Model 50 Analyzer is usable with all microprocessor families having accessible address and data busses up to 16 bits wide each. In many respects, the Model 50 is functionally equivalent to a 32-channel logic analyzer but has many additional features. It has unique search modes that find and identify the first and last instruction in a program loop. A transfer mode permits stepping forward or backward through programs without setting addresses. It can be used as a passive real time monitor or as an interactive break point generator. Other features include versatile delay modes, extensive stepping after halt capabilities, dual clock provision, $N+1/N-1$ strobe, status indicators, and more. Numerous Model 50 units may be interconnected for wider match and display, complex triggering or higher speed.

GENERAL OPERATION

The operation of the Model 50 can be described with reference to four 16 bit wide internal registers. There is a Match register, the contents of which is continually compared with the Address bus. If, after arming, a match occurs, a delay period starts. The contents of the Delay register specifies how many cycles, in the simplest case clock cycles, have to pass before a strobe signal is generated. At strobe time the momentary bit patterns of the 16 bit each Data and Address bus are latched into the Address and Data registers, and are immediately displayed on binary LEDs. If the Data bus is only 8 bits wide, the Data bus contents can be latched in two bytes at two variable strobe times to catch different microcycles, or different bytes of multibyte instructions etc. Either the clock rate or the instruction cycle rate can vary from 0 to 4 MHz and up to 8 machine cycles can be captured and displayed within an instruction cycle.

Both the Match and Delay registers can be set, reset, incremented, decremented, and displayed independently with the front panel controls. The contents of the Delay register can specify up to 65,000 clock cycle delays, instruction cycle delays, or loop delays. The loop delay specifies how many times the given match address has to be executed before strobe occurs. Also, there is a combination delay: N_1 loops followed by N_2 clocks or instruction cycles before strobe. This can be used, for example, when tracing the exit from a loop after N_1 executions. As stated, the address and data are captured at strobe time and displayed. The display can be latched to

show one-shot phenomena or it may be repeatedly strobed at a variable rate. In the latched mode, manual arming can be accomplished.

The strobe can be advanced ($N-1$) or delayed ($N+1$) by one clock cycle to trace programs, especially jumps and subroutine calls forward and backward. There is also a transfer pushbutton to load the content of the address display into the match register which permits the user to "walk through" the program branches without having to manually set the new starting addresses.

An additional feature of the Model 50 is the search mode. If a processor is hung up in a program loop the search mode can find and display the current address and instructions. Also, under normal program conditions, it will find the first and the last instructions of consecutively executed program segments. This mapping feature quickly identifies the executed sections of a program for diagnostic or verification purposes without tedious manual search. The search rate is variable. Any measurement in progress, such as a search, may be terminated by reset.

The operating modes described above are all passive. The processor has been operating at its own speed and under its own control. But there is provision, if the processor permits, to halt execution at strobe time and then to step the microprocessor and display the result under manual or variable rate automatic control. The step size can be selected as a single or multiple machine or instruction cycle, or a single or multiple loop. The single step, or $N+1$ with transfer, and search modes can be combined very effectively to trace long program segments. There is an additional user definable front panel switch position, which can operate interrupt and control lines, or can be used to select instruction cycle vs. machine cycle operation.

On the front panel, four status lights show the operating status of the Model 50. The Arm and Match lights show the "Reset", "Armed and waiting for match", "Waiting for delay", and "Measurement complete" states. The Search and Halt lights show the related conditions respectively.

A rear panel connector receives interchangeable custom wired or universal user jumperable Interface Modules. These Interface Modules adapt the Model 50 pin out to the various processors. Interchangeable cables can be used to connect the Interface Module to the processors. The easiest to use cable clips directly onto the processor chip. As an aid in hardware debugging a TTL compatible Scope Synch output pulse is provided on a rear panel BNC connector at strobe time.



Fig. 1 Model 50 Microprocessor Analyzer

The only function Logic Analyzers have over the Model 50 is the memorizing and displaying past states. In many troubleshooting cases this past memory is of questionable value. The problem either can be pinpointed, or if not, there is small probability that it will be found within the past 16 or 32 addresses or data. It is believed, that the user's interest is better served with the Model 50's new features and very low cost, less than 1/4 of the cost of comparable Logic Analyzers. However, in case someone needs it, there is provision in the Model 50 to strobe and display via an accessory RAM memory past states to any desired depth.

ARCHITECTURE OF THE ANALYZER

The heart of the Model 50 is an eight state Sequential Controller, shown on Fig. 2. Four states are indicated with the Arm and Match lights and are listed in Table I. The full state diagram and the conditions of various transitions will be described in the next chapter.

The Sequential Controller receives two timing signals from the Timing Generator. The "Synch" signal is the main clock signal and specifies the time when the Address and the Data Bus contents are in a steady state and valid. There is provision to delay the Data Strobe compared with Address Strobe. The "Beginning of Cycle" (BOC) signal is necessary to signify the start of a new machine cycle. But BOC could mean the start of an instruction cycle if so desired. Both of these timing signals are either directly available from the processor, or

ARM Lamp	MATCH Lamp	INTERNAL STATE
OFF	OFF	RESET - Analyzer will not respond to any inputs.
ON	OFF	MEASUREMENT IN PROGRESS - Analyzer is waiting for Address Match.
ON	ON	MEASUREMENT IN PROGRESS - Analyzer is waiting for Delay to time out.
OFF	ON	MEASUREMENT - is completed and displayed.

Table I Internal Operating States

they are derived from the processor's various clock and status signals by the Model 50 Timing Generator. There are five uncommitted gates brought out on the rear connector of the Model 50 to enable the Interface Module to generate the needed signals for the Timing Generator. As said before, these Interface Modules are either prewired for specific processors or are universal and user jumperable.

The Timing Generator has one more function. In case the Data Bus is not 16 bits wide, both 8 bit Data Displays are connected to the same 8 bit Bus (notice the dotted Bus line) and, in this case, the Timing Generator, in connection with the Address Strobe, will time the Display A and B Strobes to display up to 8 machine cycles within the instruction cycles. The B strobe is the variable with reference to A strobe. B has

PROCESSOR AND INTERFACE

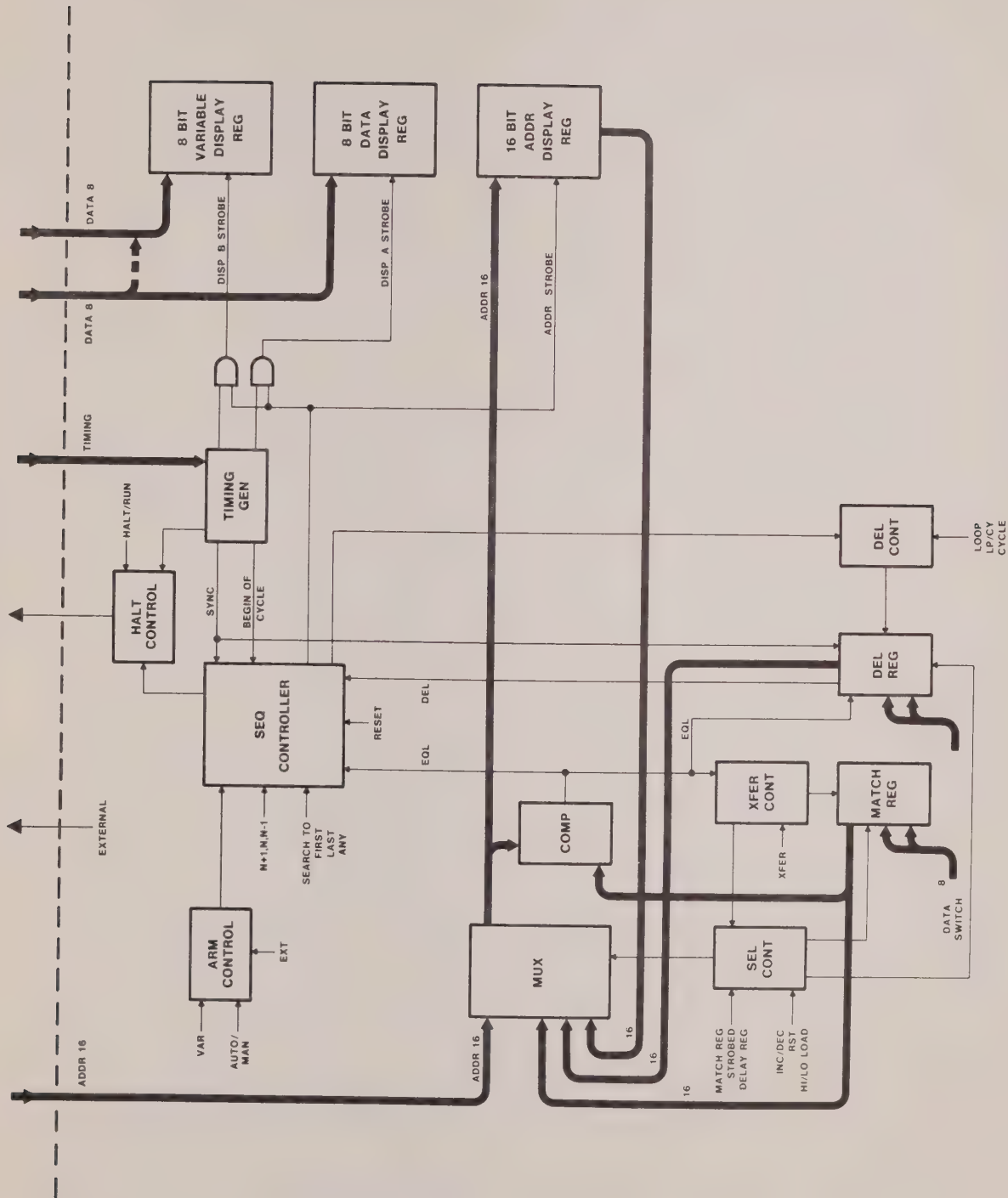


Fig. 2 Model 50 Architecture

a 9th preset position also, which is defined by appropriate jumpering on the Interface Module. Incidentally B strobe can latch any other 8 bit information, such as control signals, status lines or contents of I/O ports. The Address Bus content is always strobed into the Address Display Register at Address Strobe time, although the Address lines could also be connected to match on control or data lines.

The Sequential Controller has to be armed before any measurement is made. This can be automatic with a variable rate, or manual if one wants to study and latch one-shot phenomena. There is also a provision for external arming the Sequential Controller, which will allow the Strobe of one Model 50 to arm a second Model 50. Besides numerous manual control signals, such as N control and reset, the Sequential Controller receives two more important internal signals. One is "Equal" (EQL), a signal sent by the comparator to signify a match between the Address Bus and the internally preset Match Register; and the other is "Delayed" (DEL), a signal received from the Delay Register, meaning that a preset number of delay cycles has elapsed, or counted down to zero, after match. The Delay Register is connected to the Delay Control, which in turn receives switch closures to specify loop delay, cycle delay or loop delay followed by cycle delay. Accordingly, the Delay Register counts either synch or equal cycles or combinations. Both the Match and the Delay Registers can be preset to any 16 bit values in two 8 bit bytes via the 8 bit Address Switches and the Load switches. They can also be incremented, decremented or reset. All this is under the control of the Selection Control logic, which is connected to the three position Match Register/Strobed/Delay Register switch. In the first switch position, all the above described functions, such as loading, apply to the Match Register, and in the last switch position, to the Delay Register. In these two positions the controlled register is also displayed, via the (Mux) multiplexer, in the Address Display Register. Under these conditions no measurements take place. The Strobed position is the normal operating position, and the Address Display Register shows, also through Mux, the strobed Address Bus content.

Transfer is another operation through the Mux. It is frequently necessary to load the Match Register with the contents of the last strobed Address Display. On Logic Analyzers this requires the manual setting of 16 address switches. In the Model 50 this Transfer is a builtin function activated by the Transfer switch. The implementation is somewhat unusual. To avoid another level of Mux, the transfer is accomplished by counting up the Match Register until the comparator tells the Transfer Control that the transfer is complete.

So far all operations of the Model 50 are passive real time monitoring. However there are interactive modes available. There is an uncommitted switch marked "External". It can be used to reset, interrupt or tri-state the processor, or to simulate any other control line. Frequently it is used to change the gating of the Timing bus, thereby permitting an easy change from machine cycle operation to instruction cycles or vice versa. The other more important interactive feature is hardware breakpoint capability. If the processor per-

mits, halt can be executed at strobe time. After that, as already stated, manual or automatic, single or multiple stepping can be selected by simply selecting manual or variable rate auto arming and an appropriately delayed next breakpoint. All this is done with the Halt control logic, which receives its signal from the Sequential Controller and the Timing Generator. The Sequential Controller also outputs a strobe signal for scope synchronization or control purposes, or for arming another Model 50. But the strobe can also be used to reset or interrupt the processor, so that hardware looping can be achieved even around nonrepetitive program segments. Also by a small interrupt routine otherwise inaccessible data, such as contents of internal registers, can be examined at a breakpoint. This approach can imitate most of the features of software simulation.

STATE DIAGRAM OF THE SEQUENTIAL CONTROLLER

Figure 3 shows the eight states and all possible transitions of the Sequential Controller. The 8 states are implemented by 3 flip-flops with Q1, Q2 and Q3 outputs. Q1 and Q2 drive the Arm and Match LEDs shown in Table I. Q3 is not observable externally. As can be seen, every transition is synchronized either by SYNCH or BOC. Reset is the starting point, and ARM · SYNCH leads to the Arm state. Most typically, with strobe at N, the next state is either Display III at match time if Delay is set to zero, or Match state is followed by Display III after the Delay times out. All other states are made necessary because of N + 1 and N - 1 strobe conditions. N + 1 requires an extra cycle of Wait state, therefore (N+1) · DEL · EQU · SYNCH and (N+1) · DEL · SYNCH leads from Arm and Match to Wait respectively. The next SYNCH gives Display III.

Most complex is the N-1 strobe. Since there is no built in memory, the N-1 state can be displayed only if the Display Registers are strobed at every SYNCH in anticipation that the next cycle might be N. From Arm every (N-1) · EQU · SYNCH leads to Display I, and BOC returns it to Arm. If EQU is reached and Delay is set to zero, the next state is Finish, and the previous Display I remains. If Delay is not equal to 0, Display II is reached from Arm via N-1 · EQU · DEL. At this time, the Display II and Match states alternate until the end of the delay where (N-1) · DEL · SYNCH points to Finish again. Display III is also turned into Finish by BOC.

The three Search and the Transfer modes are also controlled by the same three flip-flops as the 8 states just discussed. In the Search modes fewer states are needed through, since N and Delay = 0 are forced regardless of the switch and Delay Register settings. N-1, N+1 or Delay ≠ 0 would give false and misleading Search displays.

The Search to Any is accomplished by forcing an EQL with an immediate strobe and display. The Search to Last checks for EQL, meaning that the instruction is executed, then increments the Match Register and checks again. Obviously this process will stop at the first branch instruction, that is at the last consecutively executed instruction. This Search is as fast as the execution of the instructions.

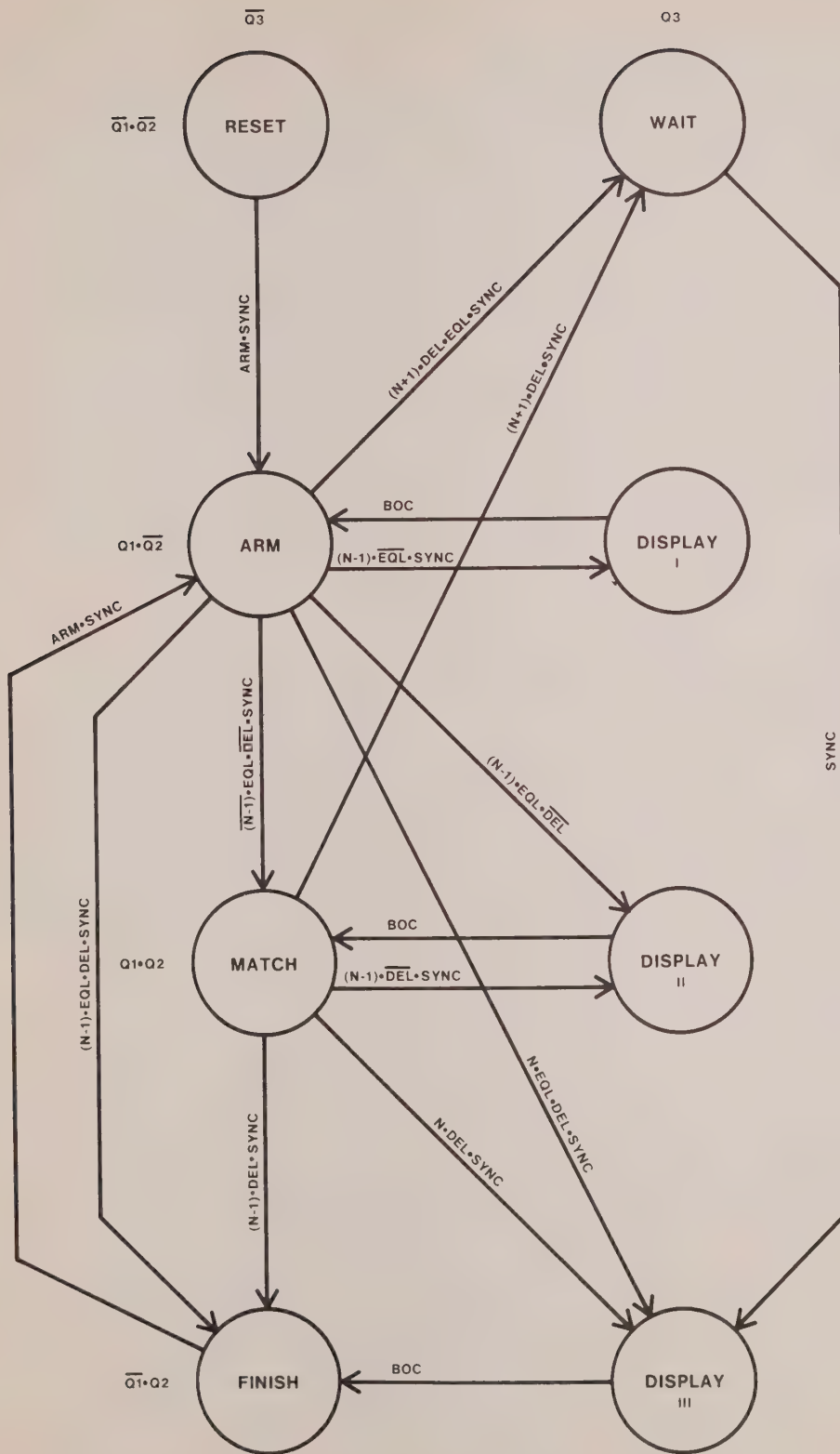


Fig. 3 State Diagram

Search to Last leaves the Search light on and has to be terminated, for example, by Transfer or Reset before normal Arming can resume. Similarly Arm has to be terminated before any Search. The restriction is rather logical: both Arm and Search lights indicate a measurement in progress. Since they are different processes, one of them has to be terminated before the other starts. The condition is stated on the front panel: SEARCH IF ARM and ARMING IF SEARCH.

The Search to First is different. Here the analyzer increments the Match Register if there is no execution. But since there is no general way to tell how long one should wait before concluding that there will be no match, the operator has to make an estimation and set the Arming Rate control for search rate timing. This is the same control, but 16 times faster, than the variable Arming rate. If the setting is in error, the worst that can happen is that the search is slower than necessary on one hand, or it is too fast and misses the first one or two instructions of the next executed program segment. This can be easily checked by manually backstepping and verifying.

APPLICATION EXAMPLE

It is quite difficult to give an adequate picture of the extensive application possibilities of the Model 50. It is somewhat like playing chess: the rules are simple but the possible strategies are almost limitless.

Let us choose a short program written for the MOS Technology 6502, assuming that the program is incorrectly or inadequately documented: a difficult but real problem. So the first task is to find out what the program is and where it is stored. Activating Search to Any gives address FFE8, there is a running program there. Search to First yields 0100. All codes will be in hexadecimal. Search to Last gives 010F. To

First again FFE0, to Last FFF2. These are therefore the only executed addresses. So far we searched in machine cycles. In instruction cycles the first address is FFE0, hence the lower addresses must be read or write addresses. Incrementing the delay in instruction cycle steps yields the code and the mnemonic interpretation of Table 2. Note that the second byte (variable at 2) sometimes shows the next instruction (in parenthesis) due to the pipelined organization of the 6502. After FFEE we loop back to FFE4. We could continue tracing the loop endlessly by incrementing delay. Decrementing instead once, at FFEE there is a branch instruction. So if we transfer this to the Match Register, reset Delay to zero, and switch to N+1, we see both branches executed at FFF0 and FFE4. After Incrementing the Match Register, N+1 shows that here we always loop back to FFE2, it is an endless loop. We can double check this: the next address is never executed, the Arm light stays on. Going back to FFE2, N-1 similarly shows two preceeding instructions: one at FFE0 the other at FFF0. Incidentally by using N+1 or N-1 and Transfer we can walk through the program forward or backward, following any branch we want.

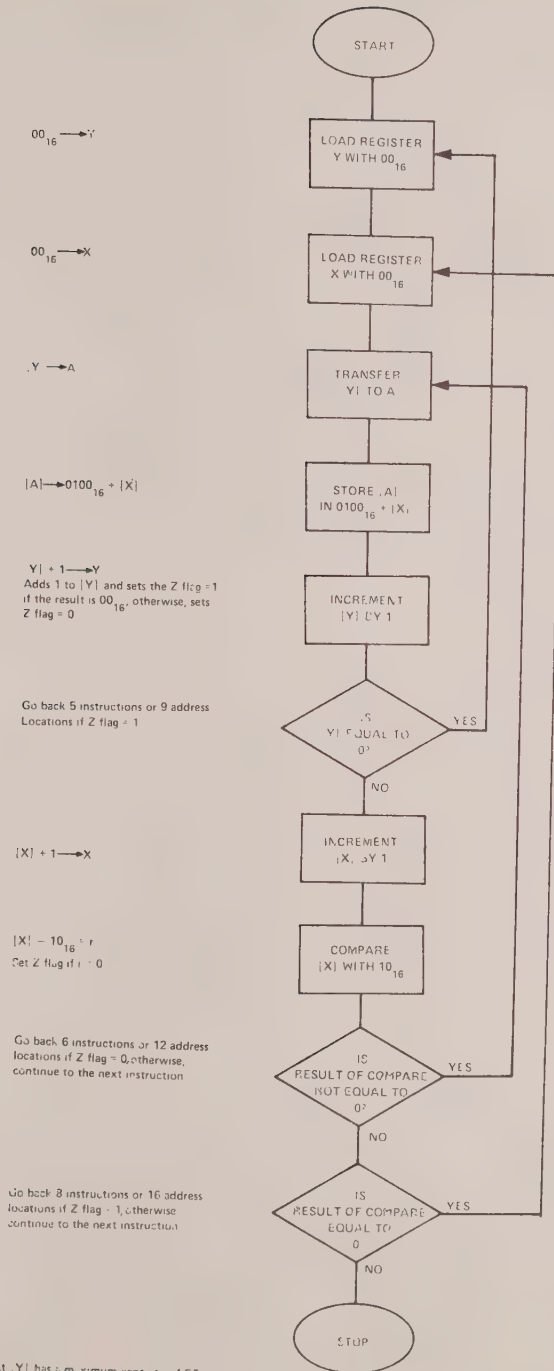
Now the program can be interpreted: it has two nested inner loops as well as a branch to the beginning from the inner most loop. The program stores in 16 locations of memory, 0100 through 010F, a successive string of numbers from 00 to FF. Thus, 16 will be added to each stored location, 16 times before the program begins again. At any of the storage addresses the high byte of the data will be counting up from 0 to F. Table III shows the write addresses and the written data. Figure 4 shows the flowchart. It is noteworthy, that the whole program can be traced without ever manually entering an Address or Delay through the Data Switches.

Hexadecimal Code		Mnemonic Code
Address	Data (Instructions)	
	First Byte 2nd & 3rd bytes if required	
FFE0	A0 00	LDY
FFE2	A2 00	LDX
FFE4	98 (9D)	TYA
FFE5	9D 00 01	STA TABLE, X
FFE8	C8 (F0)	INY
FF19	F0 F5	BFQ
FF1B	E8 (E0)	INX
FF1C	F0 10	CPX
FF11	D0 14	BNF
FFF0	F0 F0	BFQ

Table II Program Example

ADDRESS	1 DATA	2 --- 16 DATA DATA	17 DATA
0100	00	10 --- F0	00
0101	01	11	F1
0102	02	12	F2
0103	03	13	F3
0104	04	14	F4
0105	05	15	F5
0106	06	16	F6
0107	07	17	F7
0108	08	18	F8
0109	09	19	F9
010A	0A	1A	FA
010B	0B	1B	FB
010C	0C	1C	FC
010D	0D	1D	FD
010E	0E	1E	FE
010F	0F	1F --- FF	FF

Table III Data Sequence



We use the fact that |Y| has a maximum capacity of FF₁₆ and when 1 is added the result is 00₁₆ with a carry

Fig. 4 Flow Chart

Now the use of the breakpoint capability will be shown. Starting at FFE5 we can observe in the Variable window the writing of data in the 00-FF range as the fifth machine cycle. When we single arm it manually, the numbers come up randomly, we do not know whether they are written in the right place in the right order. We could reset the processor at every strobe, put the delay in loop increments and watch the data sequence properly as we increase the delay loop by loop. Or we can Halt the processor on write and single machine cycle step it 17 times with the Any/S.S. switch to see the next write. However there is a better way. Matching as before, and changing delay to five cycles, with Halt we can observe the writing of every data at every location. The processor stops every time for a period adjustable by the Arming Rate control. Or we can manually Arm and thereby step the processor in single loop, that is 7 instruction, increments very conveniently. The same result can be achieved by one lower Match Address and one higher Cycle Delay. There is a subtle reason why this is better.

If we now switch to Loops followed by Cycles Delay (LP/CY) and add 01 loop to the 06 cycle delay, this we can do with the Data Switches and Hi Load, we can see every even number stored at every even location. If we would have stayed at FFE5 with delay 5 we would have to add two loop delays for the same result, since due to pipelining the match address is executed twice per loop.

By the same reasoning if we select 0F loop delay +06 cycles, we are able to see every write execution into a selected fixed location. That is we observe one chosen row of Table III. This is equivalent of stepping in 114 instrument cycle increments without ever having to compute that number. By delaying E loops (and still the 6 machine cycles) we see the rows scanned backward, but the columns forward. By increasing the delay to FF the same data written in the same place can be observed in 1821 instruction cycle increments. By the same token FE loop delay plus 6 cycle delay scans both rows and columns backward, the program flow is seemingly reversed. There are programs which are easier to trace backward than forward.

In the above examples we observed the writing process from the main program. Instead we could match on a write address by Transfer, and delay by one machine cycle to see all writes into that address consecutively. On the other hand we can not use some of the other discussed features with this match approach.

If there is a problem all the versatility is needed frequently just to decide whether the trouble is in software, microprocessor hardware, or in the external circuitry.

We have seen some of the flexibility of a single Model 50 so far. However there is provision to interconnect any number of them. Complex trigger requirements, such as nested loops or subroutines can be easily examined if one Model 50 arms another one. For example the exit from the N_1 -th loop of a subroutine called the N_2 -th time from the N_3 -th place can be easily traced and any trouble pinpointed with two analyzers. A problem may not even exist where chain arming would be required to ten levels, but it is still good to know, that instrumentation is available.

Model 50s can also be paralleled indefinitely for wider match and wider display. Since the match can be tested on data, I/O or on control lines as well, there is another dimension of flexibility. Lastly there is provision for remote controlling every function and remote read the display of the Model 50. Under the control of a minicomputer or programmable calculator, this low cost analyzer thus could become a powerful automatic checkout tool for all microprocessor based systems. The remote controllability is a great help in the production test of the Model 50 itself, the instrument can be checked out under minicomputer control in 12 seconds.

The above examples are merely a few of the many microprocessor applications. However, the Model 50 is not necessarily limited to this field since any bus oriented system such as a minicomputer or digital control system may also be analyzed using the Model 50.

CONCLUSION

A universal Address and Data Bus Monitor has been discussed with many unique patent pending features. The architecture and operation has been covered, but space did not permit the discussion of the innumerable application possibilities. It is anticipated that this Microprocessor Analyzer, in contrast with other hardware aids, will set a new standard of low cost, flexibility and ease in software and hardware troubleshooting.

ACKNOWLEDGMENT

The author wants to thank for the numerous valuable contributions of Jon Gabel, Gary Tebbett and Jim Slater. The helpful comments of Roger Doering and Eugene Fisher are also appreciated.

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I. INTRODUCTION

The Systron-Donner Model 50 Microprocessor Analyzer* is the first of a new kind of instrument designed specifically as a low cost, software and hardware troubleshooting tool for microprocessor systems. It has the address and data display functions of a minicomputer control panel and is usable with most existing and anticipated microprocessor families.

The Model 50 Microprocessor Analyzer can be used with any system which allows external access to a Data Bus and timing lines. The timing signals are used by the Model 50 to indicate when the information on the Address and Data Bus is valid. Since the timing for different microprocessors varies, the Model 50 has been designed to accomodate a wide range of timing patterns.

II. GENERAL FEATURES

The Model 50 is a compact and lightweight bench instrument with two unibilical cables and a minicomputer like display and control panel.

ADDRESS MATCH AND DELAYS

Basically the Model 50 displays on LED's a maximum 16 bit wide address and 16 bit data or instructions in binary form. The data can be either parallel 16 bits or two consecutive 8 bit bytes. There is provision to show a third byte on three byte long instructions. The address is selectable by front panel binary switches which load an address Match Register. This register is also incremented or decremented by a switch. If, the selected address is executed by the processor, a strobe is generated at match time and the address and data are displayed. This strobe also can be delayed in one of three ways, either by a predetermined number of address matches up to 65,536 (this is useful for unravelling program loops) or by a preset number of clock cycles also up to 65,536. Among other uses, the second delay is good for tracing conditional jumps or subroutine calls. There is a combination delay as well, which allows up to 256 address matches followed by a selected number of clock cycles. This permits tracing the exit from a loop after a desired number of executions. All these delays can be reset, set, incremented, decremented, and displayed.

The address and data are captured at strobe time and displayed. The display can be latched to show one shot phenomena or can be repeatedly strobed with a variable display time. Of course, in the latched mode, there is provision for a manual arming signal.

MULTIPLE UNIT USAGE

By taking the output signals of a second Model 50 the arming can be made conditional on another address match and/or delay. Very complex triggering conditions can be set up this way by using more than one Model 50. Or two 50's can be parallel connected to display a 32 bit wide match.

*Patent Pending

STROBE CONTROL

The strobe can be advanced (N-1) or delayed (N+1) by one clock cycle to trace programs, especially jumps and subroutine calls forward and backward. There is also a transfer pushbutton. It loads the content of the address display into the match register. This permits a convenient "walking through" the program branches without having to manually set the new starting addresses.

SEARCH MODE

An additional feature is a search mode. If a processor is hung up in a program loop the search can find and display the current address and instructions. But it can be used under normal program conditions also to find the first and the last of consecutively executed program segments. This mapping feature, on the memory map, quickly identifies the executed sections of a program for diagnostic or verification purposes without tedious manual search. The search rate is also variable.

DUAL CLOCKS PROVISION

"Valid Memory Address" or "Instruction Fetch" signals can be used for the beginning of cycle indicators, while the usual clock signals are used to control machine cycles which allows subsequent 8 byte displays of multibyte instructions. Read/write or execute machine cycle operations can also be shown.

HALT AND SINGLE STEP MODE

The described operating modes so far are all passive, the processor operates at its own speed and under its own control. But there is provision, if the processor permits, to halt execution at the strobe time and then to single step and display under manual control. The single step and search modes can be combined very effectively to trace long program segments. By pushing Single Step after a jump, the next step may be read then pushing LAST the Model 50 displays the next branch point.

INTERCHANGEABLE CABLES

A rear panel connector permits interchangeable cables to be wired to the processor, clipped on to it, or to pick up the address and data bus from the memory chip. Different processors usually require different cables. An optional pod near the processor can be used for buffering and polarity inversion.

OSCILLOSCOPE SYNC OUTPUT

As an aid in hardware debugging a TTL compatible output pulse is provided on a rear panel BNC connector at strobe time. This allows viewing numerous timing signals for proper sequencing.

III. SPECIFICATIONS

Clock or Instruction Cycle Rate:	0 to 4 MHz (up to 8 machine cycles per instruction cycle).
Input Load:	Single low power Shottky TTL.
Operating Temperature:	0 to +50°C
Power:	100 to 120/200 to 240 VAC, 48 to 440 Hz, 20 W.
Interface:	Analyzer Interface Module plugs into the rear panel that adapts Data Cable to Model 50.*
Dimensions:	3.5" H X 8.375" W X 13.36" D.

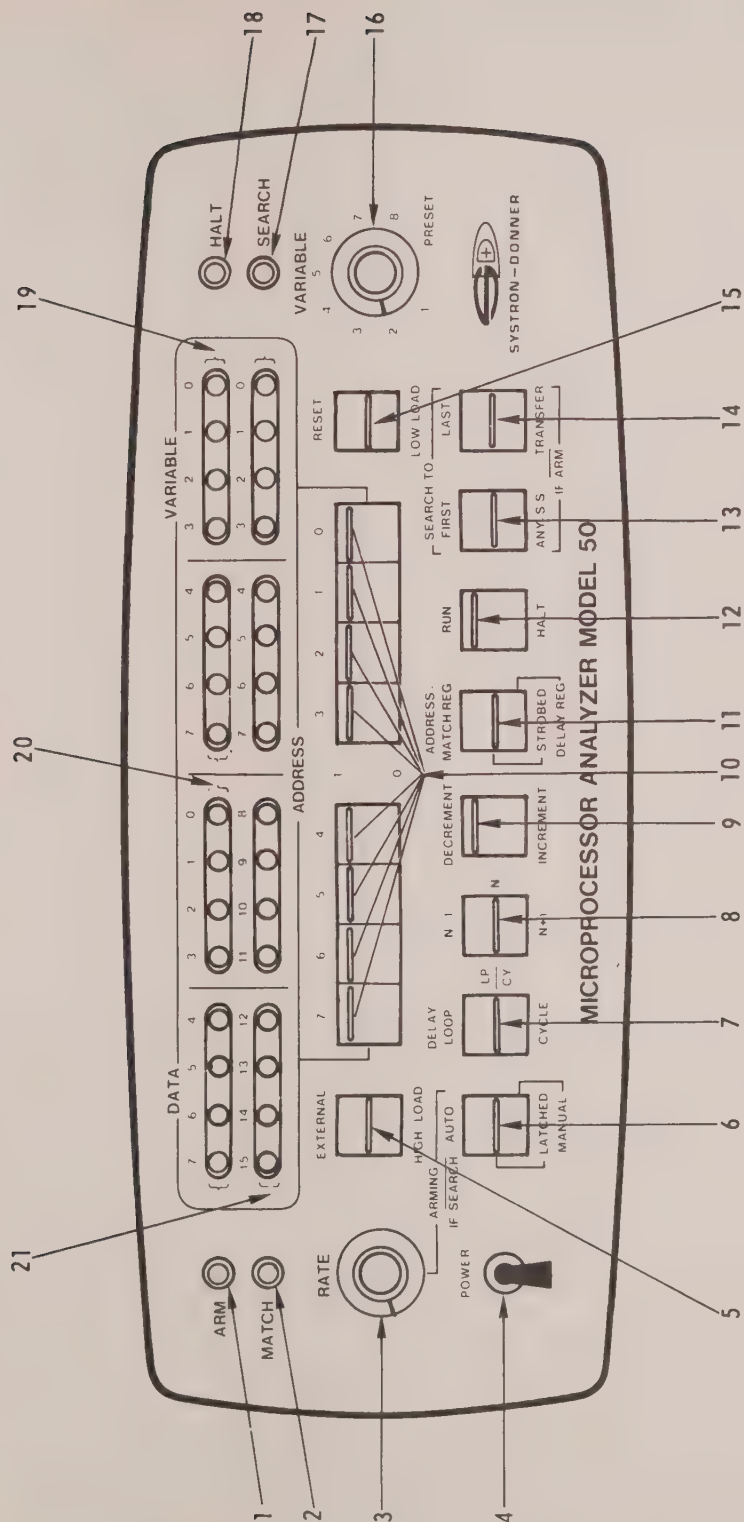
*Note: One Analyzer Interface Module and one Data Cable is required for operation, unless the Model 50 is coupled to the Demonstrator Board in which case no Interface Module is required.

Accessories Provided: One Operation and Maintenance manual and one power cord.

IV. FRONT AND REAR PANEL DESCRIPTION

FRONT PANEL, MODEL 50 MICROPROCESSOR ANALYZER (MPA)

INDEX	NAME	FUNCTION															
1	ARM (LED indicator lamp)	This indicator and the MATCH (2) indicator display the four MPA internal operating states. See table following Index 2.															
2	MATCH (LED indicator lamp)																
MODEL 50 INTERNAL OPERATING STATES																	
<table><tr><th>ARM lamp (1)</th><th>MATCH lamp (2)</th><th>MPA INTERNAL STATE</th></tr><tr><td>OFF</td><td>OFF</td><td>RESET - MPA will not respond to to any inputs.</td></tr><tr><td>ON</td><td>OFF</td><td>MEASUREMENT IN PROGRESS - MPA is waiting for Address Match.</td></tr><tr><td>ON</td><td>ON</td><td>MEASUREMENT IN PROGRESS - MPA is waiting for Delay to time out.</td></tr><tr><td>OFF</td><td>ON</td><td>MEASUREMENT is completed and displayed.</td></tr></table>			ARM lamp (1)	MATCH lamp (2)	MPA INTERNAL STATE	OFF	OFF	RESET - MPA will not respond to to any inputs.	ON	OFF	MEASUREMENT IN PROGRESS - MPA is waiting for Address Match.	ON	ON	MEASUREMENT IN PROGRESS - MPA is waiting for Delay to time out.	OFF	ON	MEASUREMENT is completed and displayed.
ARM lamp (1)	MATCH lamp (2)	MPA INTERNAL STATE															
OFF	OFF	RESET - MPA will not respond to to any inputs.															
ON	OFF	MEASUREMENT IN PROGRESS - MPA is waiting for Address Match.															
ON	ON	MEASUREMENT IN PROGRESS - MPA is waiting for Delay to time out.															
OFF	ON	MEASUREMENT is completed and displayed.															
3	ARMING - RATE (potentiometer)	This control sets the wait time before rearming occurs when the ARMING switch (6) is in the AUTO position. NOTE: ARMING control (3) and switch (6) operate only if the SEARCH (17) lamp is off (IF SEARCH). Search rate is also controled with this pot.															



FRONT PANEL, MODEL 50

FRONT PANEL MODEL 50 MICROPROCESSOR ANALYZER (MPA) (CONTD)

INDEX	NAME	FUNCTION
4	POWER (toggle switch)	This switch, in the up position, applies ac power to the primary of the power transformer in the Model 50.
5	EXTERNAL, HIGH LOAD (switch)	The EXTERNAL switch position is user defined. Typical uses are to reset or interrupt the processor, to switch in or invert timing qualifiers, or to select machine or instruction cycle delays, etc. The center position is OFF. The HIGH LOAD switch position is a momentary contact closure type with return to center which loads the ADDRESS switches (10) register contents into the most significant 8 bits of a selected register.
6	ARMING - AUTO, LATCHED, MANUAL (switch)	The AUTO switch position continuously rearms the instrument a fixed time after completing each measurement. The time delay is adjusted by the RATE, ARMING (3) control. The LATCHED switch position retains the measurement in progress until completion. The MANUAL switch position is a momentary contact closure type with return to center (LATCHED) which arms the instrument once. NOTE: ARMING control (3) and switch (6) operate only if the SEARCH (17) lamp is off (IF SEARCH).
7	DELAY: LOOP LP CY, CYCLE (switch)	The LOOP switch position causes a delay, before display, measured in processor program loops. The $\frac{LP}{CY}$ switch position causes a loop delay set by the upper 8 bits of the DELAY Register, followed by a cycle delay set by the lower 8 bits of the DELAY Register. The CYCLE switch position causes a delay measured in processor cycles.
8	N-1, N, N+1 (switch)	The N-1 switch position causes the strobed address as selected by the ADDRESS: STROBED switch (11) position to be equal to the MATCH Register contents + the DELAY Register contents -1. The N switch position causes the strobed address as selected by the ADDRESS: STROBED switch (11) position to be equal to the MATCH Register contents + the DELAY Register contents.

FRONT PANEL MODEL 50 MICROPROCESSOR ANALYZER (MPA) (CONTD)

INDEX	NAME	FUNCTION
8	(Contd)	The N+1 switch position causes the strobed address as selected by the ADDRESS: STROBED switch (11) position to be equal to the MATCH Register contents + the DELAY Register contents +1.
9	DECREMENT, INCREMENT (switch)	The DECREMENT switch position is a momentary self centering contact which subtracts one from the contents of the register selected by the ADDRESS: MATCH REG. or ADDRESS: DELAY REG. switch (11) positions and is shown in the ADDRESS display. The INCREMENT switch position is a momentary self centering contact which adds one to the contents of the register selected by the ADDRESS: MATCH REG. or the ADDRESS: DELAY REG. switch positions. The register is shown in the ADDRESS display (21).
10	ADDRESS Switch Register (switches)	These eight, two position switches allow a 0 (zero) or a 1 (one) to be entered into each of the bit positions in the eight bit register. These may be loaded into either the upper or lower 8 bits of the MATCH Register or the DELAY Register.
11	ADDRESS: MATCH REG., STROBED, DELAY REG. (switch)	The MATCH REG. switch position places the contents of the MATCH Register into the ADDRESS display (21). The register contents may then be modified by the RESET or LOW LOAD (15) switch positions as well as the HIGH LOAD (5) position or by the INCREMENT/DECREMENT (9) switch. The STROBED switch position is necessary to operate the ARMING control (3) and switch (6). The STROBED position also allows the ADDRESS display (21) to contain the results when a measurement is completed. In this position, the DECREMENT/INCREMENT switch (9) changes the Delay register. The DELAY REG. switch position places the contents of the DELAY Register into the ADDRESS display (21). The register contents may be then modified by the RESET or LOW LOAD (15) switch positions, as well as the HIGH LOAD (5) position or by the INCREMENT/DECREMENT (9) switch.

FRONT PANEL MODEL 50 MICROPROCESSOR ANALYZER (MPA) (CONTD)

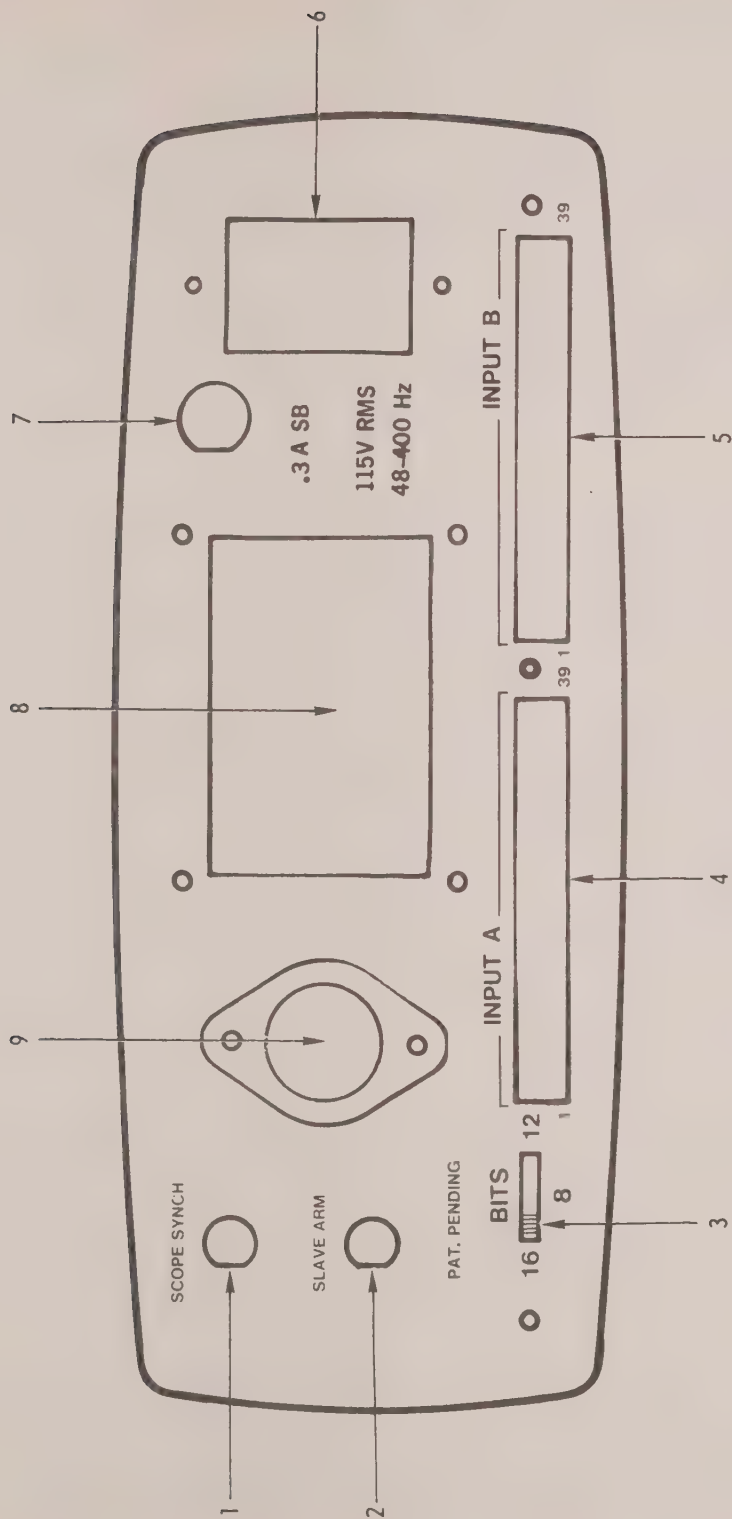
INDEX	NAME	FUNCTION
12	RUN, HALT (switch)	The RUN switch position deactivates the HALT signal. The HALT switch position activates the HALT signal to the processor at strobe time.
13	SEARCH TO: FIRST ANY/S.S. (switch)	The FIRST switch position is a momentary contact closure type with return to center which strobes the first executing address after the address in the MATCH Register. Also terminates SEARCH TO: LAST. The ANY/S.S. switch position is a momentary contact closure type with return to center which strobes the currently executing address and data. With switch (12) in HALT, ANY/S.S. single steps the processor. Also, terminates SEARCH TO: LAST. NOTE: Both SEARCH TO: switches (13) and (14) operate only if the ARM (1) lamp is off (IF ARM).
14	SEARCH TO: LAST, TRANSFER (switch)	The LAST switch position is a momentary contact closure type with return to center which strobes the last executing address after the address in the MATCH REGISTER. The TRANSFER switch position is a momentary contact closure type with return to center which places the contents of the ADDRESS display (21) into the MATCH Register. This switch also terminates a SEARCH TO: LAST (14) selection. NOTE: Both SEARCH TO: switches (13) and (14) operate only if the ARM (1) lamp is off (IF ARM).
15	RESET, LOW LOAD (switch)	The RESET switch position is a momentary contact closure type with return to center which resets the instrument, turns off the ARM (1) and MATCH (2) lamps, clears the MATCH or DELAY Registers if they are selected, and terminates a SEARCH if one is in progress. The LOW LOAD switch position is a momentary contact closure type with return to center which places the ADDRESS Switch Register (10) contents into the least significant 8 bits of a selected register.
16	VARIABLE, 1 - 8, PRESET (switch)	This nine position selector switch selects 1 through 8 processor micro-cycles; after which, the VARIABLE display (19) is loaded with whatever is on the processor Data Bus.

FRONT PANEL MODEL 50 MICROPROCESSOR ANALYZER (MPA) (CONTD)

INDEX	NAME	FUNCTION
17	SEARCH (LED indicator lamp)	This indicator is on when a SEARCH TO: FIRST, ANY/S.S. (13), LAST, TRANSFER (14) is selected and the ARM (1) lamp is off.
18	HALT (LED indicator lamp)	This indicator is on when the processor has been halted.
19	VARIABLE, 0 - 7, (LED indicator lamps)	This display is loaded at a time during the processor cycle determined by the VARIABLE, 1-8 PRESET (16) switch.
20	DATA, 0 - 7, (LED indicator lamps)	This display is an 8 bit fixed byte display which is loaded at a fixed time during the processor cycle.
21	ADDRESS, 0 - 15, (LED indicator lamps)	This display contains the address in 16 bits.

REAR PANEL MODEL 50 MICROPROCESSOR ANALYZER (MPA)

INDEX	NAME	FUNCTION
1	SCOPE SYNCH (BNC connector)	This BNC connector supplies a TTL compatible synch signal to an oscilloscope at strobe time. It may also be used to drive the SLAVE ARM BNC (2) of another Model 50 for serial triggering.
2	SLAVE ARM (BNC connector)	This BNC connector accepts an input from the SCOPE SYNCH BNC (1) of another Model 50 to allow arming after the latter has recognized a prior event.
3	BITS 16/8/12 (Slide Switch)	This switch selects the number of address bits supplied by the processor.
4	INPUT A (Ribbon Connector)	This 40 pin connector accepts one of the interface cables coupled to the microprocessor.
5	INPUT B (Ribbon Connector)	This 40 pin connector accepts one of the interface cables coupled to the microprocessor.
6	AC receptacle (Socket)	This socket accepts the three conductor power cord supplied with the Model 50.
7	FUSE (Socket)	This socket holds a 3AG .3A SLO BLO fuse for the power line.
8	POWER Transformer (Cover)	This plate covers the power transformer T1.
9	Regulator (I.C.)	This a five volt regulator for the TTL power supply.



REAR PANEL, MODEL 50

V. APPLICATION NOTE #1

INTRODUCTION

This application note demonstrates the Model 50 Microprocessor Analyzer on two programs stored in the Model 50 Demonstrator circuit board. The object of this application note is to familiarize the user with the elementary and advanced operational capabilities of the Model 50 Microprocessor Analyzer.

The Model 50 will allow real time viewing of microprocessor programs. To show this capability, the demonstrator board has been loaded with a microprocessor and two programs labeled Program 1 and Program 2. The demonstrations proceed from a simple trace routing in Program 1 to a complex multiple loop search in Program 2.

DEMONSTRATOR BOARD SETUP

The Model 50 Demonstrator Board, assembly number 057326, is a multifunction microprocessor development tool which is used to demonstrate the Model 50 Microprocessor Analyzer. This printed circuit assembly has been loaded with a MOS Technology 6502 Microprocessor, two pages of PROMs and five LS type TTL logic chips. Two switches are centered on the board for program selection.

Since the Demonstrator Board is powered by the Model 50, no separate external power supply is needed. All that is necessary for installation is to couple the two supplied ribbon cables from the rear panel of the Model 50 to the sockets on the Demonstrator Board. Make sure that INPUT A on the Model 50 is matched to INPUT A on the Demonstrator Board. The BITS switch on the Model 50 should be set to 16.

On the Demonstrator Board, Program 1 is selected with the Model 50 turned on and by setting the RST (reset) switch ON then OFF. Program 2 is selected with the Model 50 turned on and by setting the RST switch OFF and setting the NMI (nonmaskable interrupt) switch ON then OFF.

PROGRAM 1 OPERATION

Use the following procedure to operate the Model 50. Steps 1 through 3 initialize the instrument. Steps 4 through 10 demonstrate Program 1. The numbers in parenthesis refer to the front panel figure on the Foldout 1.

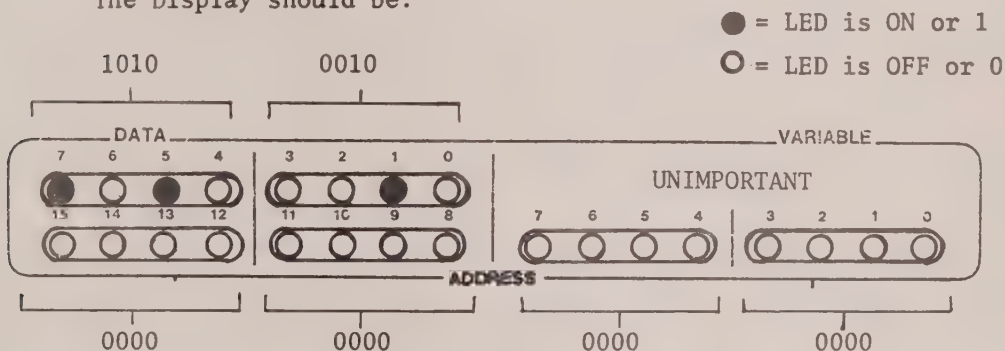
1. Plug in the supplied power cord and demonstration board cables. On the rear panel of the Model 50, set BITS switch to 16. Flip up the POWER (4) switch on the left hand side of the Model 50 front panel. Set RST switch on the Demonstrator Board ON then OFF.

If any error is made at any of the subsequent steps in this operating procedure, restart from operation step 1.

2. Set the ADDRESS: MATCH REG./STROBED/DELAY REG. switch (11) to the DELAY REG. position. Flip up the RESET/LOW LOAD momentary switch (15) to reset.

3. Set the ADDRESS: MATCH REG./STROBED/DELAY REG. switch (11) to the MATCH REG. position. Flip up the RESET/LOW LOAD momentary switch (15) to RESET.
4. Set the RUN/HALT switch (12) to the RUN position.
5. Set the DELAY: LOOP/ $\frac{LP}{CY}$ / CYCLE switch (7) to the CYCLE position.
6. Set the N-1/N/N+1 switch (8) to the N position.
7. Set the EXTERNAL/HIGH LOAD switch (5) to the EXTERNAL position.
8. Set the ADDRESS: MATCH REG./STROBED/DELAY REG. switch (11) to the center STROBED position.
9. Set the ARMING AUTO/LATCHED/MANUAL switch (6) to the AUTO position.
10. Rotate ARMING-RATE control (3) fully clockwise (fast).

The Display should be:



DATA: 1010 0010

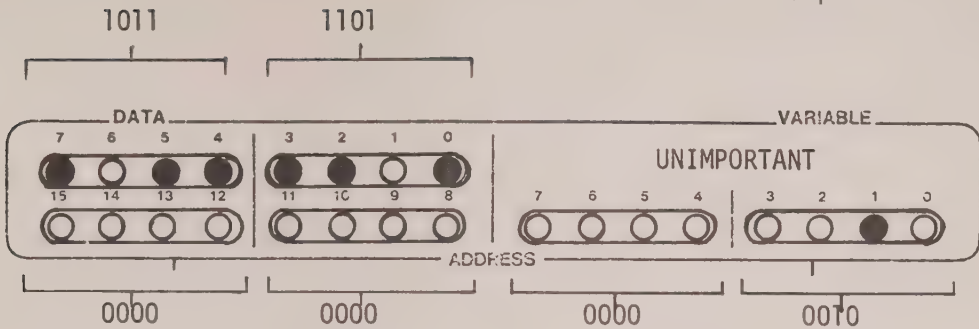
ADDRESS: 0000 0000 0000 0000

Notice that 1010 0010 is program step 0 in the Model 50 Display portion of Table 1 located on the Foldout. This data (instruction) has an address of 0000 0000 0000 0000. Only the lowest four bits of this address are listed in Table 1.

Stepping Forward Incrementing Delay

11.. The Model 50 may be made to step through the stored program by selecting INCREMENT on the DECREMENT/INCREMENT (9) momentary switch. After the first INCREMENT the display should be:

● = LED lamp is ON or 1
○ = LED lamp is OFF or 0



DATA: 1011 1101
ADDRESS: 0000 0000 0000 0010

Notice that 1011 1101 is instruction number 2 and program step 1 in the Model 50 Display portion of Table 1 located on the Foldout. This data (instruction) has an address of 0000 0000 0000 0010. Only the lowest four bits of this address are listed in Table 1.

We are now displaying program step 1 which executes instruction #2. By repeated push and release of the DECREMENT/INCREMENT switch (9) to the INCREMENT position, program steps 2 through 13 will be displayed. Notice that steps 5 through 8 of the program reexecute instructions #2 through #5. This is an interior program loop denoted by the shorter arrow in Table 1. The longer arrow is program step 13 to 14 where the program begins again at instruction #1. Thus, the processor chip on the Demonstration board is continuously executing Program 1, while the Model 50 catches and displays addresses and data of each step.

PROG STEP	INSTRUCTION NUMBER
0	1
1	2
2	3
3	4
4	5
5	2
6	3
7	4
8	5

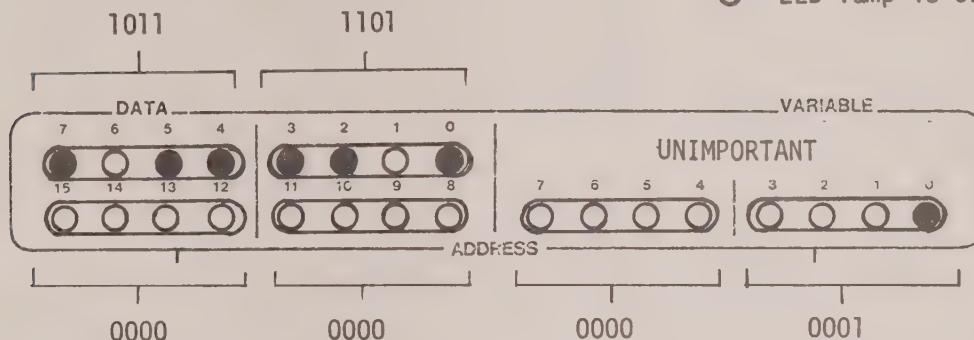
PROG STEP	INSTRUCTION NUMBER
9	2
10	3
11	4
12	5
13	6
14	1
.	.
.	.
.	.

Viewing The Program Step Number

It is possible to view, on the Model 50, the step number of the program. The 14 steps of Program 1 are numbered 0 through 13. To read the step numbers, perform the following:

12. Set ADDRESS: switch (11) to the DELAY REG. position. RESET (15) and INCREMENT (9) once. Select STROBED (11) then the DELAY REG. (11) position. The instruction 1011 1101 performed in 11. is step #1 which is displayed in the ADDRESS readout (21).

● = LED Lamp is ON or 1
○ = LED lamp is OFF or 0



DATA: 1011 1101

ADDRESS: 0000 0000 0000 0001

Incrementing the DELAY REG. (11) will display the step number. Selecting STROBED (110 shows the address and instruction. Notice that after step 13 the program loops back to address 0000₁₆ which is the beginning of the program. This will be step number 14 etc.

Stepping Backwards Decrementing Delay

13. With STROBED (11) selected, a push and release of the DECREMENT/INCREMENT switch (9) to the DECREMENT position will walk the display backwards through the program towards the Match Address.

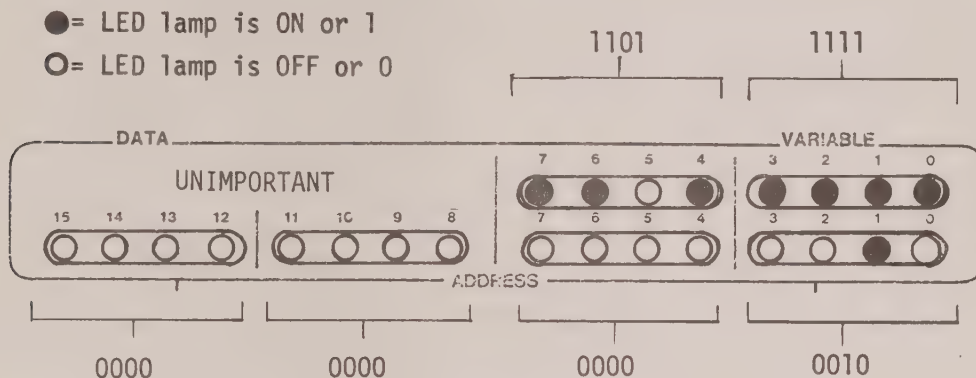
NOTE: By setting MATCH REG./STROBE/DELAY REG. switch (11) to MATCH REG. or DELAY REG. the match address or amount of delay may be checked at any time. Also, when decrementing one past 0000₁₆, the Delay Register will contain FFFF₁₆. Notice how MATCH (2) and ARM (1) LED,s have a different pattern due to the long 65,536 step delay. These two LED indicators define the internal state of the machine.

MODEL 50 INTERNAL OPERATING STATES

ARM Lamp (1)	MATCH Lamp (2)	Model 50 Internal State
OFF	OFF	RESET - Model 50 will not respond to any inputs.
ON	OFF	MEASUREMENT IN PROGRESS - Model 50 is armed and waiting for Address Match.
ON	ON	MEASUREMENT IN PROGRESS - Model 50 has a match and is waiting for Delay to time out.
OFF	ON	MEASUREMENT is completed and displayed.

Viewing Multi-Byte Instructions

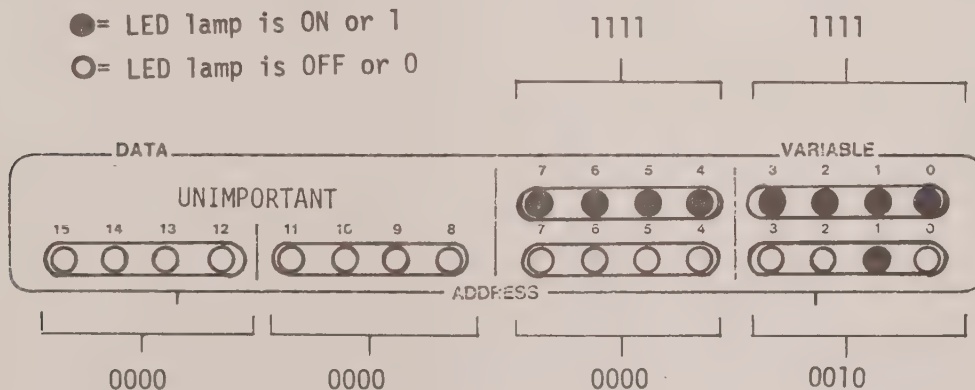
14. Select DELAY REG. (11), RESET (15), INCREMENT (9), and STROBED (11). Set VARIABLE switch (15) to the 2 position. The VARIABLE display (19) should read:



VARIABLE: 1101 1111 ADDRESS: 0000 0000 0000 0010

The VARIABLE display (19) now shows the second byte of the instruction at address 0000 0000 0000 0010.

15. Set the VARIABLE switch (16) to the 3 position. The VARIABLE display (19) should read:



VARIABLE: 1111 1111

ADDRESS: 0000 0000 0000 0010

By repeating operation steps 1. through 11. and selecting position 2 or 3 on the VARIABLE rotary switch (16), the 2nd or 3rd bytes of all the instructions can be displayed in the VARIABLE data display (19).

NOTE: For this application, the VARIABLE DATA latch input is in parallel with the normal DATA latch input to copy the microprocessor Data Bus. However, this latch can be used to monitor any 8 bit signal i.e., I/O Port, control lines, status lines, etc.

Viewing Known Branch Points

To view branch instruction #6 at address 0000 0000 0000 1011 perform the following:

16. Select DELAY REG. (11) and set the ADDRESS switches to 0000 0000.
17. Flip down the EXTERNAL/HIGH LOAD switch (5) to the HIGH LOAD momentary position and release. This stores 00_{16} in the two high address bytes of the Delay Register.
18. Flip down the RESET/LOW LOAD switch (15) to the LOW LOAD momentary position and release. This stores 00_{16} in the two low order bytes of the Delay Register.
19. Select MATCH REG. (11).
20. Flip down the EXTERNAL/HIGH LOAD switch (5) to HIGH LOAD and release. This puts 00_{16} in the two high order bytes of the Match Register.
21. Set the ADDRESS switches (10) to 0000 1011 and flip down the RESET/LOW LOAD switch (15) to LOW LOAD and release. This stores 0000 1011 in the two low order bytes of the Match Register.
22. Set ARMING-IF SEARCH switch (6) to AUTO. Set ADDRESS: switch (11) to STROBED. The Model 50 Display should read:

```
DATA:      1111 0000
ADDRESS: 0000 0000 0000 1011
ARM:       OFF
MATCH:     ON
```

23. Set N-1/N/N+1 switch (8) to N+1.

The Address display will alternate between 0000 0000 0000 0010 (0002_{16}) and 0000 0000 0000 1100 ($000C_{16}$). This indicates when the Branch Not Equal (BNE) at address 0009_{16} is executed. If executed, the N+1 address past the pointer (Match Address $000B_{16}$) is 0002_{16} . If not executed, the N+1 address past the pointer (Match Address $000B_{16}$) is $000C_{16}$. Adjust ARMING-RATE control (3) for best viewing time.

Stepping Forward Moving Match Address

To walk through Program 1 execution by moving the Match Register rather than incrementing the Delay Register perform the following:

24. Select MANUAL (6) until 0000 0000 0000 0010 (0002_{16}) is shown in the ADDRESS display. Select TRANSFER (14). Now repeat MANUAL (6) and TRANSFER (14) to walk through the program by moving Match Register.

Notice that branch instructions will take more than one byte for execution and as a result, the fetch and move involved in the branch will take multiple steps. Therefore the stepping forward will stop at the first branch.

Stepping Backwards Moving Match Address

25. Select N-1 (8). Select TRANSFER (14) then MANUAL (6). Now repeat TRANSFER (14) and MANUAL (6) to walk backwards through Program 1 by moving the Match Register.

Stepping backwards will pass through a branch without stopping, unlike the stepping forward procedure.

$03_{16} \rightarrow X$

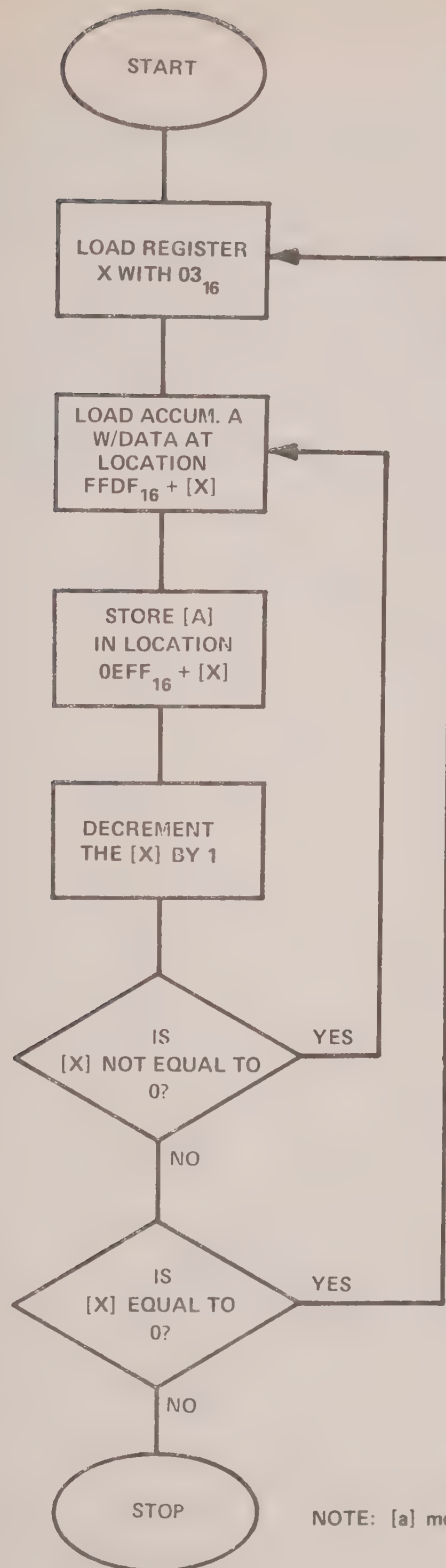
$[FFDF_{16} + [X]] \rightarrow A$

$[A] \rightarrow 0EFF_{16} + [X]$

$[X] - 1 \rightarrow X$ and if $[X]$ is 0 the Z flag is set

If Z flag is not set, go back 3 instructions or 8 address locations, otherwise, continue to the next instruction

If the Z flag is set, go back 5 instructions or 12 address locations, otherwise, continue to the next instruction



NOTE: [a] means the contents of a.

PROGRAM 1 FLOW CHART

The sample program given in Table 1 takes the contents of three (3) consecutive storage locations in memory and reads them one by one into the main processor register (ACCUMULATOR) and stores them one by one into three (3) consecutive new memory locations. All this takes place on the demo board, the Model 50 in this configuration only monitors the operation of the microprocessor.

Figure 1 shows the front panel of the Microprocessor Analyzer Model 50. The panel is rectangular with rounded corners. At the top, there are two main sections: 'DATA' on the left and 'VARIABLE' on the right. Each section contains eight indicator lights arranged in two rows of four. Below these sections is a large 'ADDRESS' display area with a grid of lights. To the left of the panel, there are four controls: 'AMP' (a small knob), 'MATCH' (a small knob), 'RATE' (a large knob), and 'POWER' (a large knob with a power symbol). To the right, there are three controls: 'MULT' (a small knob), 'SEARCH' (a small knob), and 'VARIABLE' (a large knob). Below these controls is a 'SYSTEM-POWERED' logo. The panel is labeled with various text elements, including 'DATA', 'VARIABLE', 'ADDRESS', 'MULT', 'SEARCH', 'VARIABLE', 'ANALYST', and 'SYSTEM-POWERED'. Numbered callouts 1 through 18 point to various components and labels on the panel.

TABLE 1. SAMPLE PROGRAM 1

Model 50 Display

Program Step	Instr. #	Binary Code							
		Address *	Data (Instructions)		Variable (Instructions)		Variable (Instructions)		
		(lowest 4 bits)	First byte		Second byte		Third byte		
0 14	1	0000	1010	0010	0000	0011			
1 5 6	2	0010	1011	1101	1101	1111	1111		
2 9 10	3	0101	1001	1101	1111	1111	0000	1110	
3 7 11	4	1000	1100	1010					
4 8 12	5	1001	1101	0000	1111	0111			
5 13	6	1011	1111	0000	1111	0011			

18

PROGRAM 2 OPERATION

To operate the Model 50 with Program 2, turn on the Model 50 and set the Demonstrator Board switches as follows:

RST - ON then OFF

NMI - ON then OFF

The Program description is on Foldout Number 2. The numbers in () refer to the front panel callouts shown on Foldout Number 1.

LOCATE PROGRAM OPERATING AREAS

To locate where the program is operating perform the following:

1. Set RATE (3) to fast full clockwise, Select MATCH REG. (11) then RESET (15) and DELAY REG. (11) then RESET (15).
2. Select EXTERNAL OFF (center position) (5), LATCHED (6), CYCLE (7), N (8), STROBED (11), RUN (12).
3. Select ANY/S.S. The Model 50 then searches to any executed address and displays one address where the processor is operating.
4. Selecting FIRST (13) yields 0000 0001 0000 (0100₁₆). Selecting LAST (14) yields 0000 0001 0000 1111 (010F₁₆). These are two other operating areas of Program 2.

STEPPING FORWARD INCREMENTING DELAY

To step through Program 2 by incrementing the delay register, perform the following:

5. Set FFE0₁₆ into the MATCH REG. (11) with the ADDRESS switches (10) and RESET (15) the DELAY REG. (11) to 0000₁₆.
6. Set RATE (3) to fast c.w. Select EXTERNAL (5), AUTO (6), CYCLE (7), N (8), STROBED (11), and RUN (12).

Each time INCREMENT (9) is selected and released, the Model 50 will step to the next executed instruction.

WATCH EVERY WRITE INTO EVERY LOCATION

To view every write into every location executed by Program 2, perform the following:

7. Set MATCH REG. (11) to FFE4₁₆ and the DELAY REG. (11) to 0006₁₆ using the ADDRESS switches (10).
8. Set RATE to slow, c.c. Select EXTERNAL OFF (5), AUTO (6), $\frac{LP}{CY}$ (7), N (8), STROBED (11), HALT (12).

For each of the sixteen addresses called, there are sixteen different entries displayed before the program recycles to the beginning. The DATA contains the written information and the ADDRESS contains the location where it is written.

WATCH EVERY WRITE INTO SELECTED LOCATION

9. Set RATE (3) fast, c.w. Select MANUAL (6) until the address location to be viewed is displayed.
10. Set DELAY REG. (11) to $0F06_{16}$ using the ADDRESS switches (10).
11. Set RATE to slow, c.c. Select AUTO (6) and STROBED (11).

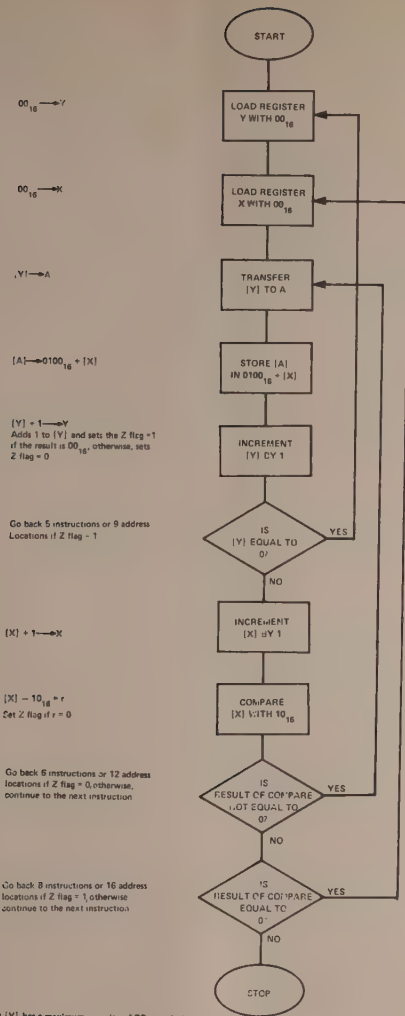
The DATA display shows the writes into the selected address location. To verify these writes, we can view the m from the location in which they are written instead of from the main program.

12. Select TRANSFER (14). This places the address of the selected location into the Match Register.
13. Set DELAY REG. (11) to 0001_{16} . Select STROBE (11). The writes should show in the DATA display.

BINARY CODED HEX DISPLAY

Microprocessors operate in HEXadecimal computer code. The instructions, the address, and the data all are coded in HEX (base 16). The microprocessor itself converts the HEX code into a binary representation of this code. The Model 50 displays this binary representation of the HEX number.

Decimal	Binary Bit Position				Hex Symbol
	3	2	1	0	
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
10	1	0	1	0	A
11	1	0	1	1	B
12	1	1	0	0	C
13	1	1	0	1	D
14	1	1	1	0	E
15	1	1	1	1	F



We use the fact that (Y) has a maximum capacity of FF₁₆, and when 1 is added the result is 00₁₆ with a carry.

PROGRAM 2, FLOW CHART

PROGRAM 2 DESCRIPTION

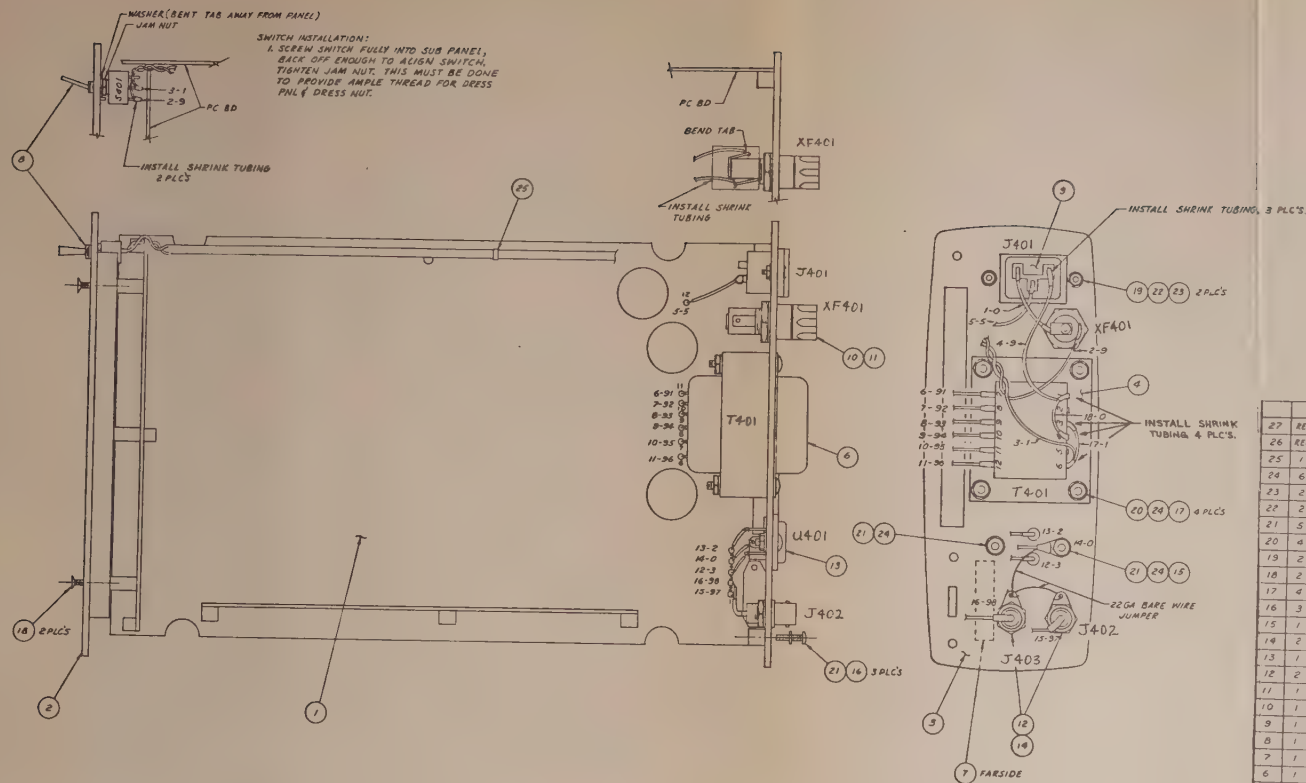
Program 2 has two nested inner loops as well as a branch to the beginning from the inner most loop. The program stores in 16 locations of memory, 0100₁₆ through 010F₁₆, a successive string of numbers from 00 to FF₁₆. Thus, 16₁₆ will be added to each stored location, 16 times before the program begins again.

ADDRESS	1 DATA	2- - - - - DATA	16 DATA	17 DATA
0100	00	10- - - - -	F0	00
0101	01	11	F1	
0102	02	12	F2	
0103	03	13	F3	
0104	04	14	F4	
0105	05	15	F5	
0106	06	16	F6	
0107	07	17	F7	
0108	08	18	F8	
0109	09	19	F9	
010A	0A	1A	FA	
010B	0B	1B	FB	
010C	0C	1C	FC	
010D	0D	1D	FD	
010E	0E	1E	FE	
010F	0F	1F- - - - -	FF	

At any of the storage addresses the high byte of the data will be counting up from 0 to F₁₆. See steps 9. through 13. of the application note.

TABLE 2 PROGRAM 2

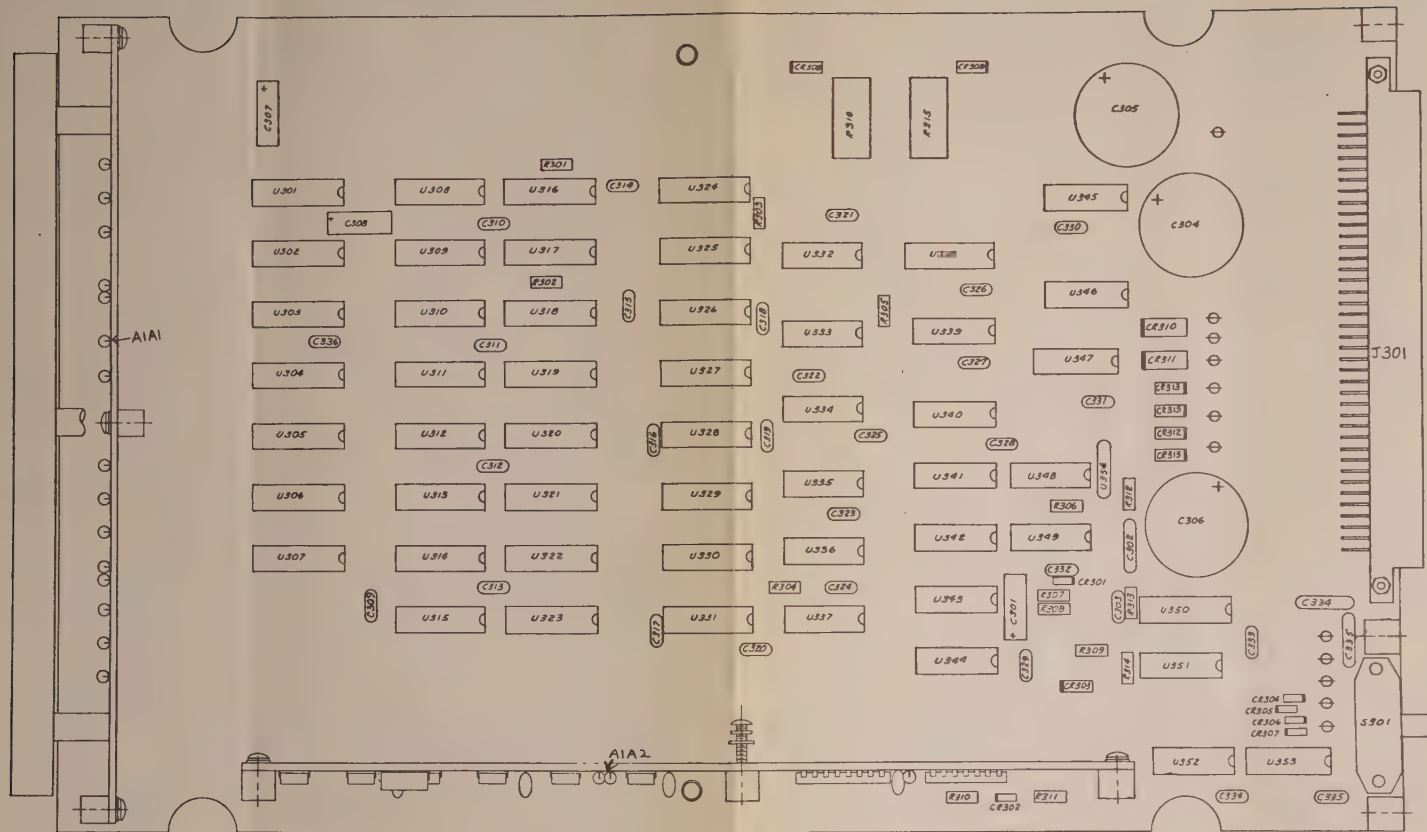
Hexadecimal Code			Mnemonic Code
Address	Data (Instructions)		
	First Byte	2nd & 3rd bytes if required	
FFE0	A0	00	LDY
FFE2	A2	00	LDX
FFE4	98		TYA
FFE5	9D	00 01	STA <u>TABLE</u> , X
FFE8	C8		INY
FFE9	F0	F5	BEQ
FFEB	E8		INX
FFEC	E0	10	CPX
FFEE	D0	F4	BNE
FFF0	F0	F0	BEQ



27	REF	9A057371	ITP	
26	REF	70037371	SCHEMATIC	
25	1	100753	CABLE TIE	
24	6	100882	NUT #6 KEP	
23	2	100341	NUT #8 KEP	
22	2	100703	WASHER #8 FLAT	
21	5	10063207	SCREW 6-32 x 7/16 PHM	
20	4	10063222	SCREW 6-32 x 1/8 PHM	
19	2	10062607	SCREW 4-40 x 1/4 PHM	
18	2	10072010	SCREW 4-40 x 5/8 PHM	
17	4	100704	WASHER #6 FLAT	
16	3	100712	WASHER #8 SPLIT	
15	1	100609	SOLDER LUG #8	
14	2	107077	BMC BND LUG	
13	1	025787	IC LM309K	U401
12	2	101155	BMC	J402, J403
11	1	100610	FUSE .3A SB 3AG	F401
10	1	102409	FUSE POST 3AG	XF401
9	1	101288	AC RECEPTICAL	J401
8	1	103985	TOGGLE SWITCH	S401
7	1	A037112	FOIL CAL NAME PLATE	
6	1	A04561761	END BEL	
5	1	A057284	TEST ASSY WIRE LIST	
4	1	B057139	POWER TRANSFORMER	T401
3	1	C057203	REAR PANEL	
2	1	C057205	SUB PANEL	
1	1	D057202	WIRE LIST	A1

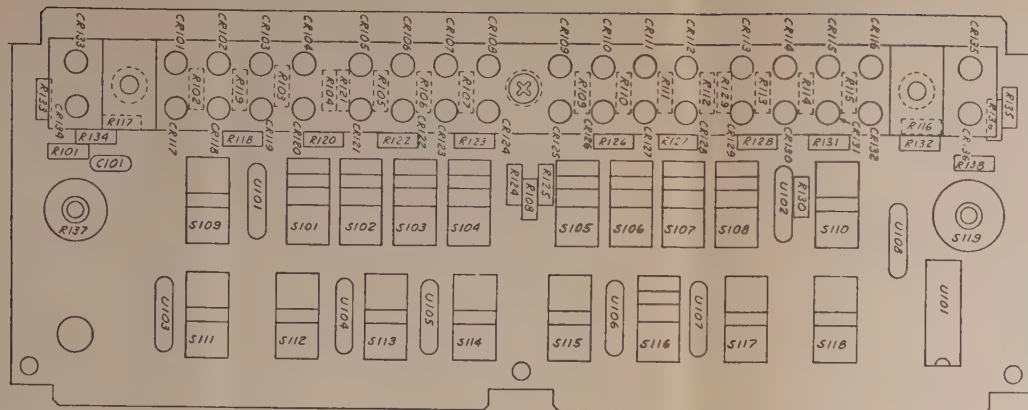
MODEL 50
TEST ASSEMBLY

#057371 REV A



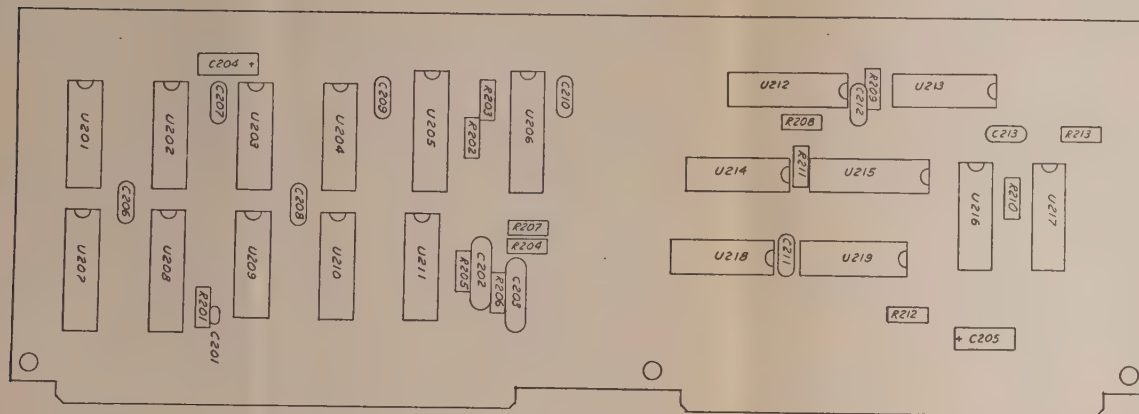
A1, LOGIC P.C. ASSEMBLY

05728201 REV A



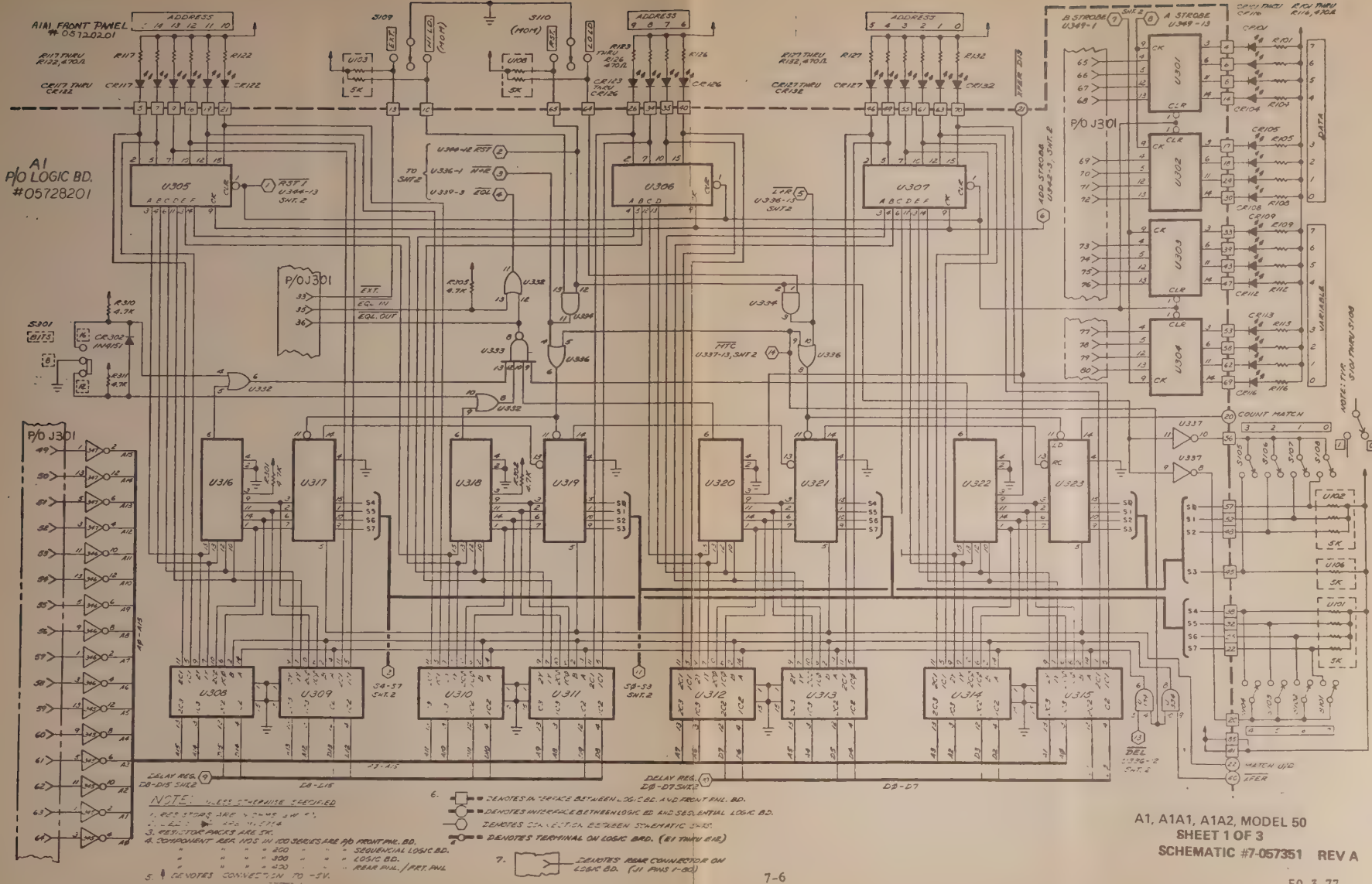
A1A1, FRONT PANEL
P.C. ASSEMBLY

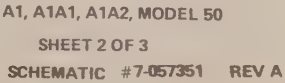
05720201 REV A

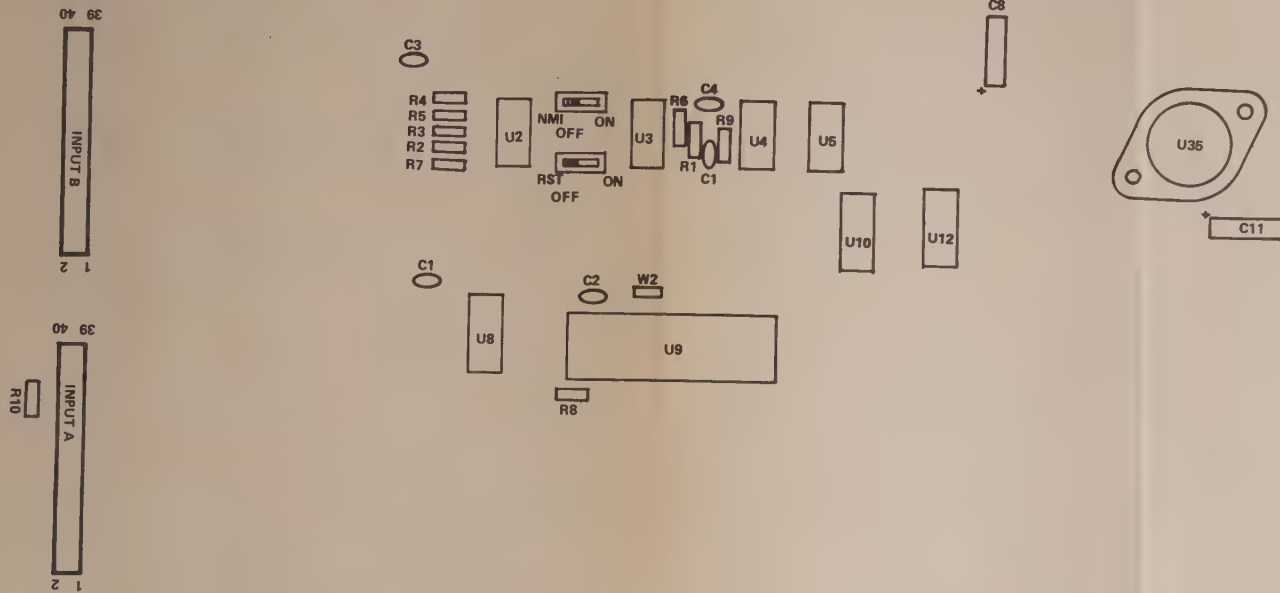


A1A2, SEQUENTIAL LOGIC
P.C. ASSEMBLY

05725201 REV A







MODEL 50 DEMONSTRATOR BD
ASSEMBLY

MODEL 50 UNIVERSAL TIMING REQUIREMENTS

GENERAL

All inputs and internal circuitry in the Model 50 are edge triggered.

The Model 50 requires four basic input timing events (Some may be coincident). These are:

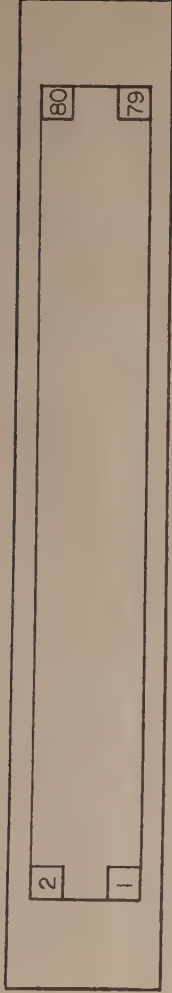
1. Beginning or end of Processor Cycle or instruction cycle (BOC),
2. When ADDRESS is valid - to be compared with match register,
3. When DATA A is valid - to be strobed into display marked DATA on the Front Panel, and
4. When DATA B is valid - marked VARIABLE on the Front Panel.

To aid in generating these strobes, the following circuits are provided:

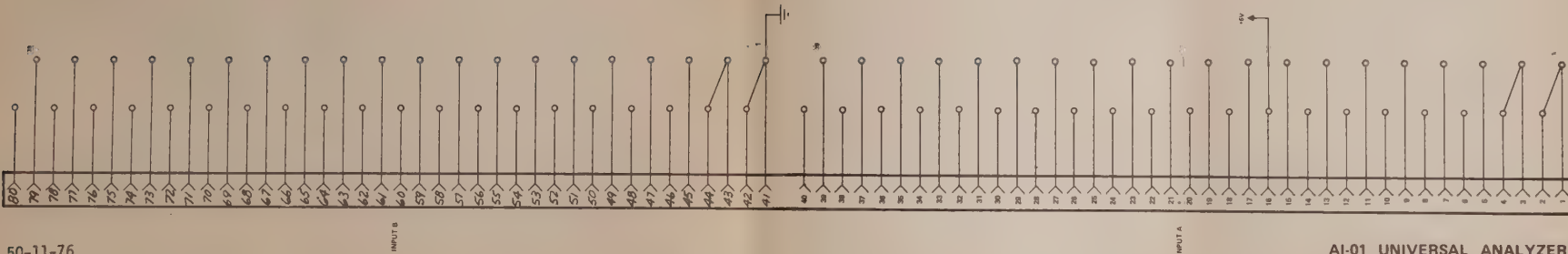
1. ANDed leading edge and trailing edge inputs of the beginning of cycle (BOC) one-shot,
2. An 8 bit shift register to count down a basic clock frequency (Cleared at BOC),
3. Positive, ANDed inputs on the "SYNC" (Address Valid) strobe, and Display 'A' and Display 'B' (Data Valid Strobes).
4. 5 uncommitted gates to condition processor signals to supply the above input signals.
5. 'External' switch line - Closure to GND when pushed up to select different operating modes ie. machine cycle vs instruction cycle or control external functions from the 50 front panel. Used to reset or interrupt the processor.

Also available on the Rear Panel connector are:

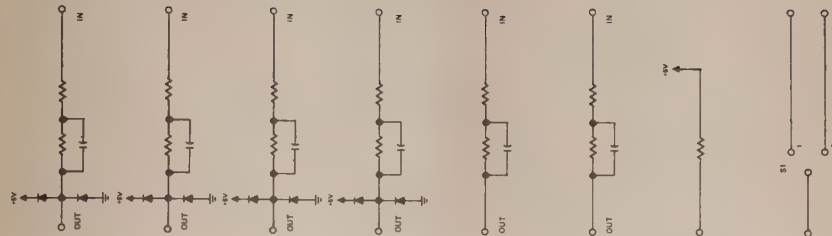
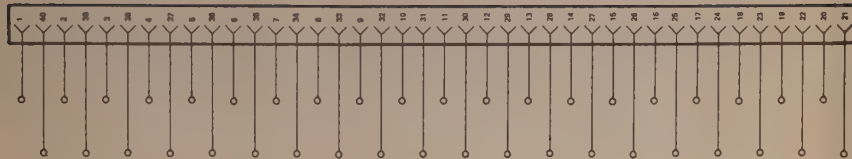
- EQL IN - Normally grounded, used in multiple Model 50 operation for 32, 48, etc, Bit Address Match.
- EQL OUT - Normally open, used for 32, 48, etc Bit Match.
- HALT QUAL - Used to synchronize Halt condition with processor timing.
- CONT QUAL - Used to SYNC start up from Halt with processor timing.
- HALT - Used to Halt processor.
- BOC QUAL - Permits BOC after HALT. In most applications should be connected to HALT (pins 31 and 30 jumpered).
- SLAVE ARM - Used for Multiple 50 hookups and to ARM the 50 remotely.
- REG +5 - to be used for pull up resistor for Rear Panel ONLY..
- SCOPE SYNC - Same signal as available on BNC. Can be connected to slave arm other 50's for chain armed operation.
- FLOATING POWER SUPPLY - Filtered, Unregulated $\pm 10\text{Vdc}$ nominal.



REAR PANEL CONNECTOR



AI-01 UNIVERSAL ANALYZER
INTERFACE MODULE SCHEMATIC



APPLICATION NOTE

AI-8080

The AI-8080 Analyzer Interface is designed for the Intel 8080 and 8080A Microprocessors. 8080 devices produced by other manufacturers will also work with this interface; however, differences exist which may require varying the operating or electrical characteristics of the Interface. If the user experiences any Interface difficulty, the Systron-Donner Instrument Division will provide assistance. Phone (415) 676-5000 Ext. 265 for help.

Operational modifications of the Model 50:

Set VARIABLE switch to the 1 or PRESET position.

Set BITS switch to 16.

Delay and single or multiple stepping will be executed in machine cycle increments. To halt execution at strobe time, the microprocessor READY pin 23 is pulled low by Model 50 connector pin 7. Any other drive to the READY pin 23 should be tri-state or open collector with a light pull-up resistance of 3.3 k Ω or greater. If an 8224 Clock Generator and Driver chip is driving the READY pin 23, a resistor may be serially inserted into that line so that, with the DC-03 clip, the Model 50 controls the READY line; otherwise, without the clip, the 8224 chip controls the READY line. For convenience, a complement signal is available at the Model 50 connector pin 12.

APPLICATION NOTE

AI-8080X

The AI-8080X Analyzer Interface has been designed according to the published specifications of the Intel 8080 and 8080A microprocessors. Other 8080 type processors produced by other manufacturers have also been successfully tested with this interface though they are not always hardware and software compatible with the Intel 8080 or with each other. If the user experiences any Analyzer Interface difficulty with a non-compatible device, the Systron-Donner Instrument Division will provide assistance: phone (415) 676-5000, Ext. 265.

Operational set-up of the Model 50:

Set VARIABLE switch to the 1 position to display status bits.

Set BITS switch to 16.

Cycle Delay and single or multiple stepping will be executed in machine cycle increments if the EXTERNAL switch is in the EXTERNAL position and in instruction cycle increments if the switch is in the center position. To halt execution at strobe time, the microprocessor READY pin 23 is pulled low or HOLD pin 13 pulled high by the Model 50. The user must choose one of these pins and put the supplied insulating sleeve on the other pin of the DC-03 cable. Any other drive to the READY pin 23 or HOLD pin 13 should be tri-state or open collector with a light pull-up resistance of 6.8 k Ω or greater. If a low impedance source such as a TTL totem pole output is driving these pins, a 6.8k or greater resistor may be serially inserted into those lines so that both the Model 50 with the DC-03 clip and the μ p system without the DC-03 clip may control the READY or HOLD lines.

Alternatively, if the user has access to the READY or HOLD pins through another chip, such as the 8224 clock chip or an inverter, a separate clip lead may be used from pins 8 (HALT) or 9 (HALT) of the 74LS04 chip on the AI-8080X to the appropriate input. The additional delay caused by this indirect control should be less than 20 ns.

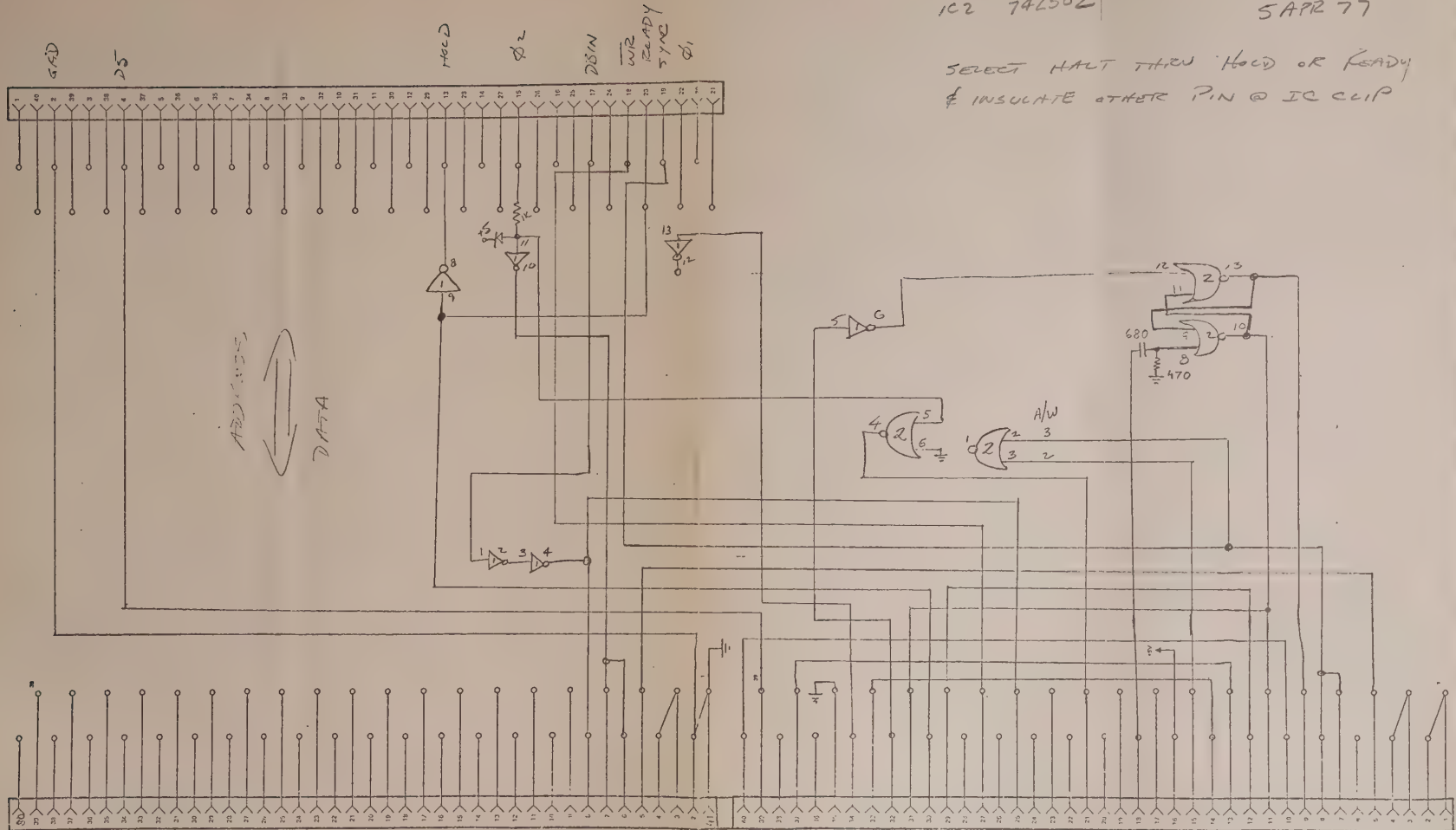
The AI-8080X has a clamp to reduce the processor clock undershoot to acceptable levels. If, however, large clock undershoot ($>1V$) exists on 02 at pin 15 of the 8080 μ p, some form of clamping or damping should be used to prevent incorrect strobing.

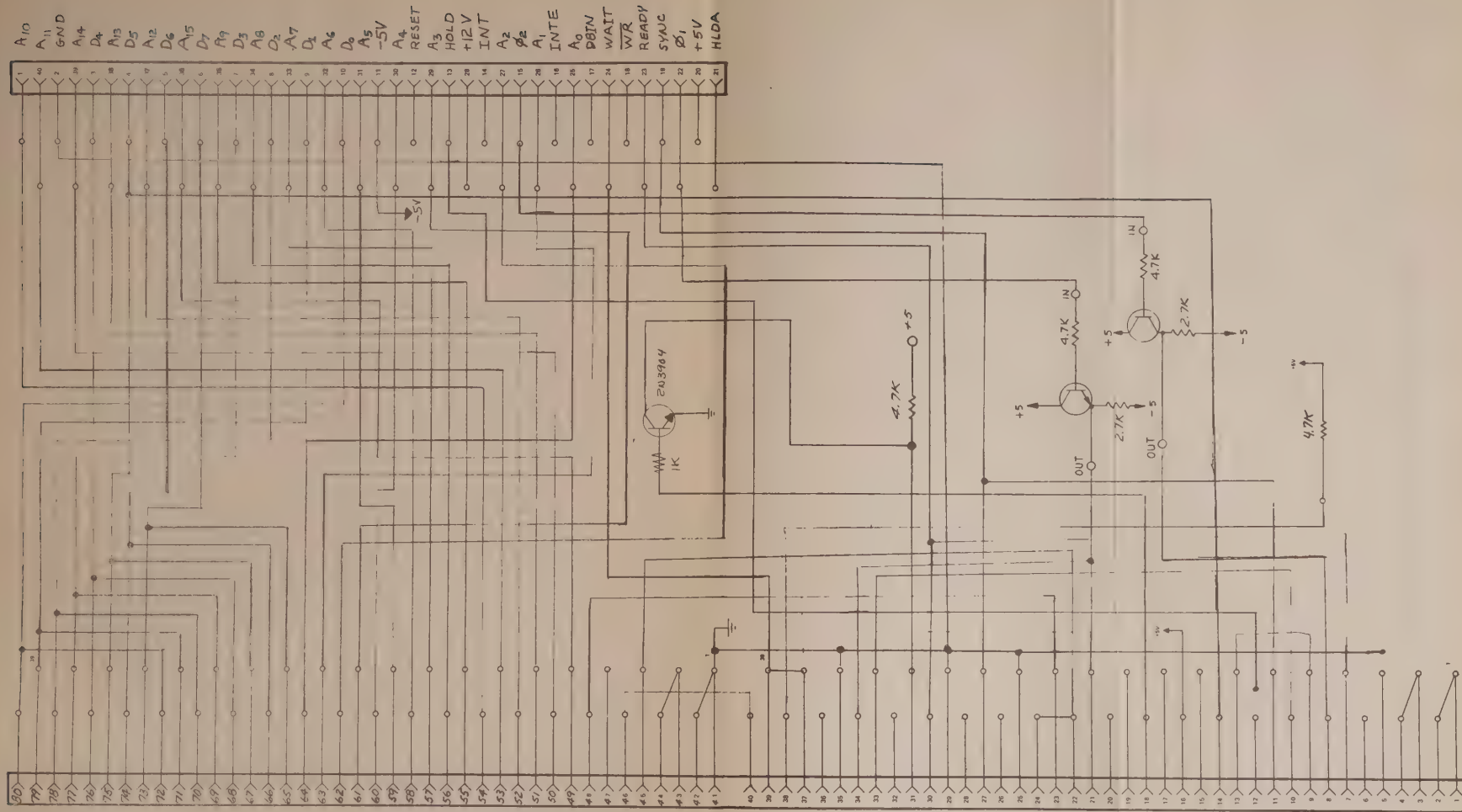
Note that SEARCH TO-FIRST or ANY/S.S. can be done in either machine cycles or instruction cycles. SEARCH TO-LAST, however is valid in machine cycles only.

IC1 74LS04
IC2 74LS02

AI-8080X
5 APR 77

SELECT HALT THEN HOLD OR READY
INSULATE OTHER P/N @ IC CLIP





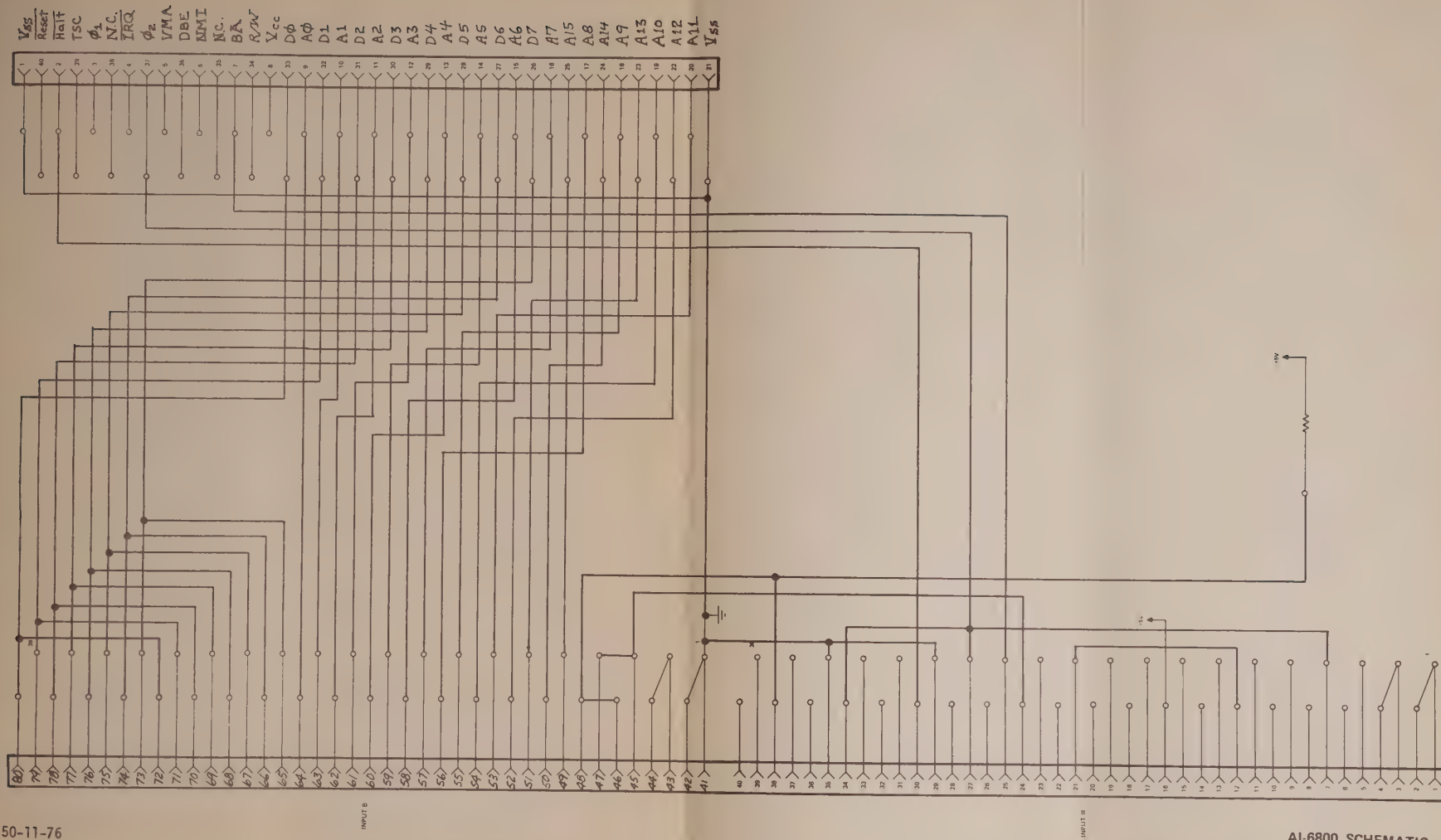
APPLICATION NOTE

AI-6800

The Analyzer Interface module for the 6800 microprocessor unit is designated AI-6800.

Operational modifications for the Model 50.

Set BITS switch to 16.



CHAPTER 6

REPLACEABLE PARTS

6.1 INTRODUCTION

This chapter contains the spare parts lists for each assembly in the Model 50. Ordering information is included and should be used when purchasing parts from the factory. Explanation of the column listings and Table 6.1 Manufacturers Code-To-Name index are also included.

6.2 PART ORDERING INFORMATION

To order a part from the Replaceable Parts List, state the Systron-Donner part number, indicate the quantity required and address the order to the nearest Systron-Donner sales or service center.

To order a part not listed in the Replaceable Parts List, state the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Systron-Donner Sales or Service center.

6.3 PARTS LISTS

Table 6.1 gives the code-to-name information for the manufacturers listed in the replaceable parts lists. The replaceable parts lists are placed in a numbered sequence.

Each column in the parts lists provide specific information relating to the listed parts as follows:

- (1) **DESIGNATOR:** Item and Reference numbers applicable to assemblies. Reference numbers are listed in alpha-numeric order.
- (2) **COMPONENT NOMENCLATURE AND DESCRIPTION:** Component names and specifications are provided in these columns and include; value, tolerance, wattage rating, working voltage, construction, etc.
- (3) **MANUFACTURER'S CODE:** H4-2 Federal Supply Code numbers are listed to identify component manufacturers. A Manufacturers Index is provided in this chapter for cross-reference.
- (4) **MANUFACTURER'S PART NUMBER:** True manufacturer part numbers are listed in this column.
- (5) **SD STOCK NUMBER:** The Systron-Donner stock number is listed in this column.
- (6) **T/Q (Total Quantity):** This quantity, appearing after an item entry, indicates the number of times the component is used in that assembly. The total quantity for each part is given only once – at the first appearance of the part number in the list.

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION		TEST ASSEMBLY 057371				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		TEST ASSEMBLY	52542	057371	057371	1
1	A1	LOGIC P.C. ASSEMBLY	52542	05728201	05728201	1
11	F401	FUSE, 3AGSB, .3A 250V	75915	323.300	100610	1
9	J401	CONNECTOR POWER, Male Ch.	82389	EAC-301	101288	1
12	J402	RECEPTACLE, RF BNC UG1094/U	83456	UG-1094/U	101155	2
12	J403	Same as J402				
8	S401	SWITCH, Toggle SPDT GA250V	OHTO	FTD41-BLK	103985	1
4	T401	TRANSFORMER POWER	52542	057139	057139	1
13	U401	I.C., Voltage Regulator 5V1A 20W	27014	LM309K	025787	1
2		SUB PANEL	52542	057205	057205	1
3		REAR PANEL	52542	057208	057208	1
6		END-BELL, Transformer	52542	04561761	04561761	1
7		FOIL CAL NAME PLATE	52542	037112	037112	1
14		LUG SOLDER	79963	814	107077	2
15		LUG SOLDER #4	83330	1416-4	100509	1
16		SPLIT LOCK #6	96906	MS35338-136	100712	3
17		FLAT WASHER #6	96906	MS15795-805	100704	4
18		SCREW, FHMS 4-40 x 5/8	96906	MS24693-C7	10072010	2
19		SCREW, PHMS 4-40 x 1/2	96906	MS51957-17	10062608	2
20		SCREW, PHMS 6-32 x 1 1/2	96906	MS51957-36	10063224	4
21		SCREW, PHMS 6-32 x 1/2	96906	MS51957-30	10063208	5
22		WASHER #4	96906	MS15795-803	100703	2
23		NUT KEP 4-40	78187	511-041800-00	100941	2
24		NUT KEP 6-32	78189	511-061800-00	100862	6
25		CABLE TIE	06383	SST2S	100753	1

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION MODEL 50, SHIPPING ASSEMBLY 057422

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		SHIPPING ASSEMBLY	52542	057422	057422	1
		SERVICE MANUAL	52542	M-50	M-50	1
		CORD, Line, 8' 3 x 18 NEC, IEC	70903	BR-1736	102407	1
		NUT, Bezel Dress	09353	B7099	100893	1
		FOOT BUMPER, Rubber	77969	4460	103880	4
		KNOB, Dial Skrt, Black	08730	C1016-2-A-INDEX	117088	1
		BAIL, 5¼ in. Stainless Steel	52542	057132	057132	1
		FOOT	52542	057064	057064	4
		DECORATIVE PANEL	52542	057209	057209	1
		BOTTOM COVER	52542	057261	057261	1
		TOP COVER	52542	057260	057260	1
		WINDOW, Display 32 POS	52542	057218	057218	1
		WINDOW, Display 2 POS	52542	057226	057226	2
		WASHER, #6 Split	96906	MS35338-135	100711	2
		WASHER, #6 Flat	96906	MS15795-805	100704	2
		SCREW, 6-32 x 3/8 PHMS	96906	MS51957-28	10063206	2
		SCREW, 6-32 x 5/8 PHMS	96906	MS51957-31	10063210	4
		SCREW, 6-32 x 1 5/8 PHMS		By Description	10063226	4
		NUT, 6-32 Small Pattern	96906	NAS671C6	100638	4
	SEP P/L	TEST ASSEMBLY	52542	057371	057371	1

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION <u>A1, LOGIC PC ASSEMBLY</u> #05728201						
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	A1	P.C. BOARD LOGIC	52542	057282	057282	1
	A1A1	P.C. Assembly, Front Panel	52542	05720201	05720201	1
	A1A2	P.C. Assembly, Sequential Logic	52542	05725201	05725201	1
	C301	CAPACITOR, Tant 39 μ F 10V 10%	56289	150D396X9010B2	100183	2
	C302	CAPACITOR, Ceramic 1 μ F 50V 20%	56289	5CZ5U105X0050C5	100176	3
	C303	CAPACITOR, D Mica 5 pF 500V .5 pF Tol	72136	DM15CD050D0	100218	1
	C304	CAPACITOR, El Can 5000 μ F 15V	99392	23C15TS53	106459	3
	C305	Same as C304				
	C306	Same as C304				
	C307	CAPACITOR, Tant 56 μ F 6V 10%	56289	150D566X9006B2	100225	1
	C308	Same as C301				
	C309 thru C333	CAPACITOR, Ceramic .01 μ F 100V +80 - 20%	91418	TA110	100103	26
	C334	Same as C302				
	C335	Same C302				
	C336	Same as C309				
	CR301	DIODE, Signal 50V	03508	1N4151	100385	6
	CR302	Same as CR301				
	CR303	DIODE, Signal 40V 80mA	52542	006700	006700	1
	CR304	Same as CR301				
	CR305	Same as CR301				
	CR306	Same as CR301				

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION <u>A1, LOGIC PC ASSEMBLY #05728201 (Cont)</u>						
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	CR307	Same as CR301				
	CR308	DIODE, Rect. 600V 1A	04713	1N4005	100413	
	CR309	Same as CR308				
	CR310	DIODE, Rect. 50V 3A	81483	30S05	103252	2
	CR311	Same as CR310				
	CR312	Same as CR308				
	CR313	Same as CR308				
	CR314	Same as CR308				
	CR315	Same as CR308				
	R301	RESISTOR, CC 4.7K 5% 1/4W	01121	CB4725	101598	12
	R302	Same as R301				
	R303	Same as R301				
	R304	Same as R301				
	R305	Same as R301				
	R306	Same as R301				
	R307	RESISTOR, CC 100Ω 1/4W 5%	01121	CB1015	101609	1
	R308	RESISTOR, CC 47k 1/4W 5%	01121	CB4735	101574	1
	R309 thru R314	Same as R301				
	R315	RESISTOR, CC 36 Ω 5% 2W	01121	HB3605	106046	2
	R316	Same as R315				
	S301	SWITCH, Slide 1P3T PC Mount	79727	GI-153-0001C	117059	1

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION A1, LOGIC PC ASSEMBLY #05728201 (Cont)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	U301	I.C., TTL MSI Quad D-F/F	01295	SN74LS175N	103981	5
	U302	Same as U301				
	U303	Same as U301				
	U304	Same as U301				
	U305	I.C., TTL MSI Hex D-F/F W/Clear	01295	SN74LS174N	103980	2
	U306	Same as U301				
	U307	Same as U305				
	U308	I.C., TTL MSI Dual 4 To 1 Linc MUX	01295	SN74LS153N	103978	8
	U309 thru U315	Same as U308				
	U316	I.C., TTL MSI 4 Bit Magtd Cmpr	01295	SN74LS85N	103974	4
	U317	I.C., TTL MSI Syn Bin Up/Down Cntr	01295	SN74LS191N	103982	8
	U318	Same as U316				
	U319	Same as U317				
	U320	Same as U316				
	U321	Same as U317				
	U322	Same as U316				
	U323	Same as U317				
	U324	Same as U317				
	U325	I.C., TTL SMI Syn 4 Bit Cntr	01295	SN74LS163N	103979	4
	U326	Same as U317				
	U327	Same as U325				
	U328	Same as U317				

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION A1, LOGIC PC ASSEMBLY #05728201 (Cont)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	U329	Same as U325				
	U330	Same as U317				
	U331	Same as U325				
	U332	I.C., TTL SSI Quad 2—In OR Gate	01295	SN74S32N	103973	2
	U333	I.C., TTL SSI Dual 4—In NAND Gate	01295	SN74S20N	106638	1
	U334	I.C., TTL SSI Quad 2—In AND Gate	01295	SN74LS08N	103967	2
	U335	I.C., TTL SSI 8—In NAND Gate	01295	SN74LS30N	103971	1
	U336	I.C., TTL SSI Quad 2—In OR Gate	01295	SN74LS32N	103972	1
	U337	I.C., TTL SSI Hex Inv <20NS	01295	SN74LS04N	103749	4
	U338	I.C., TTL MSI Dual 4 To 1 Line MUX	01295	SN74S153N	117057	1
	U339	I.C., TTL SSI Quad 2—In NOR Gate	01295	SN74S02N	103966	2
	U340	I.C., TTL SSI Quad 2—In NAND Gate	01295	SN74S00N	025785	
	U341	I.C., TTL SSI Quad 2—In AND Gate	01295	SN74S08N	117058	1
	U342	Same as U340				
	U343	Same as U332				
	U344	Same as U334				
	U345 thru U347	Same as U337				
	U348	Same as U340				

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION <u>A1, LOGIC PC ASSEMBLY #05728201 (Cont)</u>						
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/O
	U349	Same as U339				
	U350	I.C., TTL SSI Dual Retrigger One Shot	01295	SN74LS123N	103976	1
	U351	I.C., TTL MSI 8 B Ser In Par Out	01295	SN74LS164N	103396	1
	U352	I.C., TTL SSI Quad 2 In NAND Gate	01295	SN74LS00N	103130	1
	U353	I.C., TTL SSI Quad 2 In NOR Gate	01295	SN74LS02N	103367	1
	U354	RESISTOR, Module 4-5k 20% Comp Carbon	52542	027867	027867	1
	J301	CONNECTOR, PC Edge	17235	VPB01B40A00A1G	117079	1
		SCREW, 4-40 x 9/16 PHMS		By Description	10062609	2
		SPACER, Rectangular 6-32	88245	1590 B	100489	3
		SPACER, Rectangular 4-40	88245	1591 B-11	101090	6
		SPACER, Swage 6	71279	1247-9	100517	2
		SCREW, 4-40 x 3/8	96906	MS51957-15	10062606	6
		WASHER #4 Split	96906	MS35338-135	100711	8
		WASHER #4 Flat	96906	MS15795-803	100703	8
		NUT, #4 Hex	96906	MS35649-244	100707	2
		TERMINAL	88245	2000B	100482	12

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION A1A1, FRONT PANEL PC ASSEMBLY #05720201

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/O
	A1A1	P.C., Board Front Panel Model 50	52542	057202	057202	1
	C101	CAPACITOR, Ceramic .01 μ F 100V +80-20%	91418	TA110	100103	1
	CR101-136	DIODE, Led Red	50522	MV5754	103960	36
	R101-136	RESISTOR, CC 470 Ω 5% 1/4W	01121	CB4715	101625	36
	R137	RESISTOR, Variable 250k 10%	01121	WP2G106P254BA	103927	1
	R138	RESISTOR, CC 4.7k 5% 1/4W	01121	CB4725	101598	1
	S101-108	SWITCH, Toggle S PDT	09353	7101 J2J3 CBE	103952	9
	S109	SWITCH, Toggle 1 P3POS ON OFF ON	09353	7107 J29V3 CBE	117062	1
	S110	SWITCH, Toggle	09353	7105 J29V3 CBE	117063	1
	S111	SWITCH, Toggle 1P ON OFF ON	09353	7107 J2V3 CBE	103955	1
	S112	SWITCH, Toggle 1P3POS ON ON ON	09353	7211 J2V3 CBE	103956	1
	S113	SWITCH, Toggle 1P On OFF ON	09353	7103 J2J3 CBE	103953	1
	S114	SWITCH, Toggle	09353	7215 J29V3 CBE	117060	1
	S115	SWITCH, Toggle	09353	7211 J29V3 CBE	117061	1
	S116	Same as S101				
	S117	SWITCH, Toggle 1P3POS On On On	09353	7215 J2V3 CBE	103957	1
	S118	SWITCH, Toggle 1P (ON) OFF ON	09353	7105 J2V3 CBE	103954	1

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION <u>A1A1, FRONT PANEL PC ASSEMBLY #05720201 (Cont)</u>						
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	S119	SWITCH, Rotary 1P 9 POS	01686	11-FCB-9-PC	103959	1
	U101	I.C., TTL SSI Hex Inv 15V Open Col	01295	SN7416N	045230	1
	U102-109	RESISTOR Module 4 - 5k .1W 20% Comp Carbon	52542	027867	027867	8
		SPACER Swage 4 - 40	06540	9537B-B-0440-3A	100024	3
		SUPPORT, LED Model 50	52542	057307	057307	1
		BLOCK, Annunciator Model 50	52542	057219	057219	1
		SCREW 4-40 x 5/8 FHMS	96906	MS24693-C7	10072010	1

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION <u>A1A2 SEQUENTIAL LOGIC PC ASSEMBLY #05725201</u>						
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	A1A2	P.C. Board Sequential Logic	52542	057252	057252	1
	C201	CAPACITOR Ceramic Mold 1000pF 50V 20%	71590	CW15C102M	100251	1
	C202	CAPACITOR D Mica 1500 pF 500V 5%	72136	DM19FD152JO	100150	2
	C203	Same as C202				
	C204	CAPACITOR Tant 39 μ F 10V 10%	56289	150D396X9010B2	100183	2
	C205	Same as C204				
	C206 thru C213	CAPACITOR Ceramic Disc .01 μ F 100V +80-20% Same as C206	91418	TA110	100103	8
	R201	RESISTOR CC 100 Ω 5% 1/4W	01121	CB1015	101609	3
	R202	RESISTOR CC 4.7k 5% 1/4W	01121	CB4725	101598	8
	R203	Same as R202				
	R204	Same as R201				
	R205	RESISTOR CC 300 Ω 5% 1/4W	01121	CB3015	101537	2
	R206	Same as R201				
	R207	Same as R205				
	R208 thru R213	Same as R202				
	U201	I.C. TTL SSI Quad 2-In AND Gate	01295	SN74LS08N	103967	3
	U202	I.C. TTL SSI Quad 2-In OR Gate	01295	SN74LS32N	103972	2

REPLACEABLE PARTS LIST

EQUIPMENT/ASSEMBLY DESIGNATION A1A2 SEQUENTIAL LOGIC PC ASSEMBLY #05725201 (Cont)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/O
	U203	I.C. TTL SSI Quad 2-In NOR	01295	SN74S02N	103966	1
	U204	I.C. TTL SSI Triple 3-In NAND	01295	SN74LS10N	103968	2
	U205	I.C. TTL SSI Dual J-K Flip Flop	01295	SN74S112N	025786	2
	U206	I.C. TTL MSI 8 To 1 Line Mux	01295	SN74S151N	103977	1
	U207	I.C. TTL MSI Quad $\bar{S}/\bar{R}$ Latches	01295	SN74LS279N	117056	1
	U208	I.C. TTL MSI Quad $\bar{S}/\bar{R}$ Latches	01295	SN74279N	103983	1
	U209	I.C. TTL SSI Quad 2 INPUT NAND Gate	01295	SN74S00N	025785	1
	U210	I.C. TTL SSI Quad 2-INPUT NAND Gate	01295	SN74LS00N	103130	1
	U211	I.C. TTL SSI Hex Inverter <2 ONS	01295	SN74LS04N	103749	1
	U212	Same as U205				
	U213	Same as U201				
	U214	I.C. TTL SSI Quad 2 In NOR	01295	SN74LS02N	103367	1
	U215	I.C. TTL MSI Sync Binary Up/Down Counters	01295	SN75LS193N	103162	1
	U216	I.C. TTL SSI Quad 2-Input OR	01295	SN74S32N	103973	1
	U217	Same as U201				
	U218	I.C. TTL SSI Dual 4-Input AND	01295	SN74LS21N	103970	1
	U219	Same as U204				

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